Development of Monolithic Pixel Detectors for ATLAS

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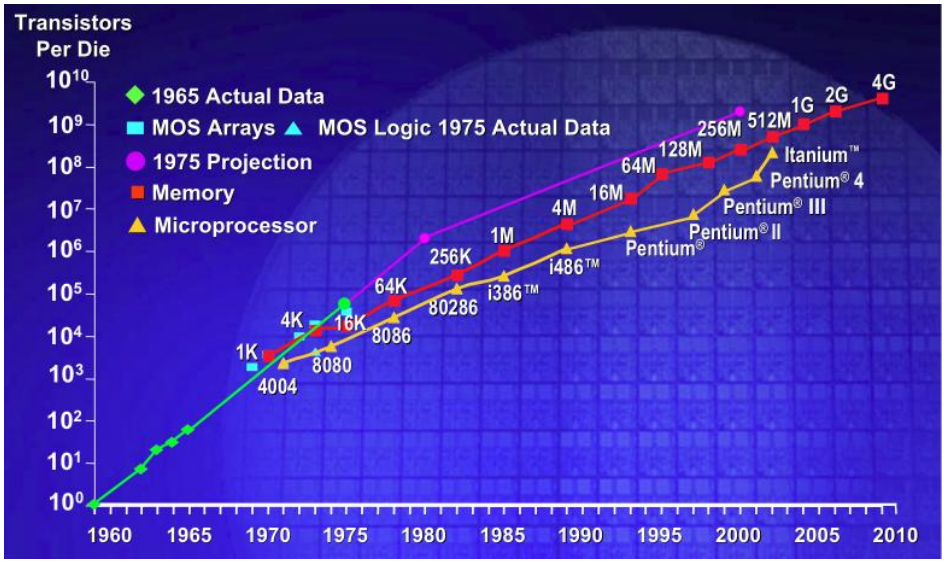
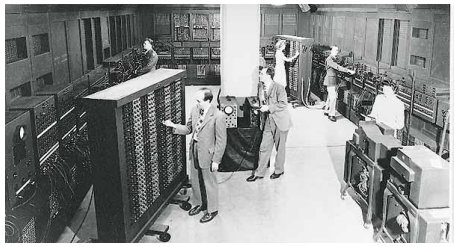
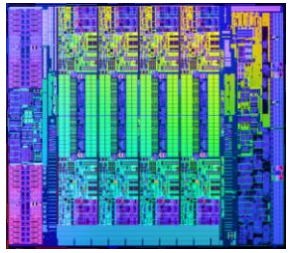
IFAE

Silicon, a history of success

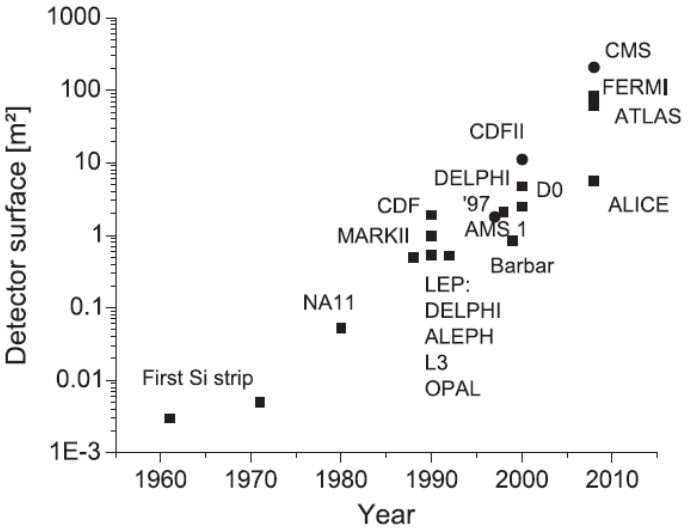


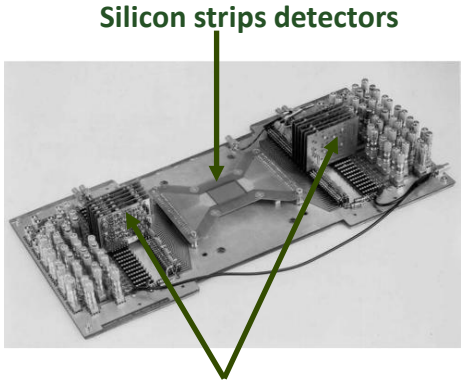


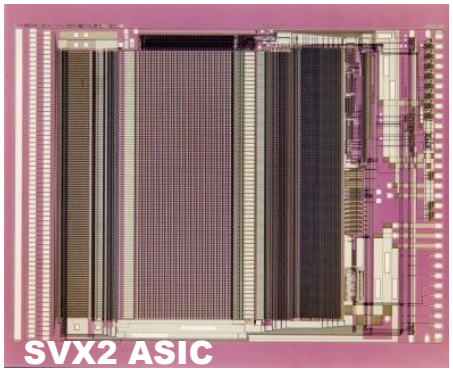


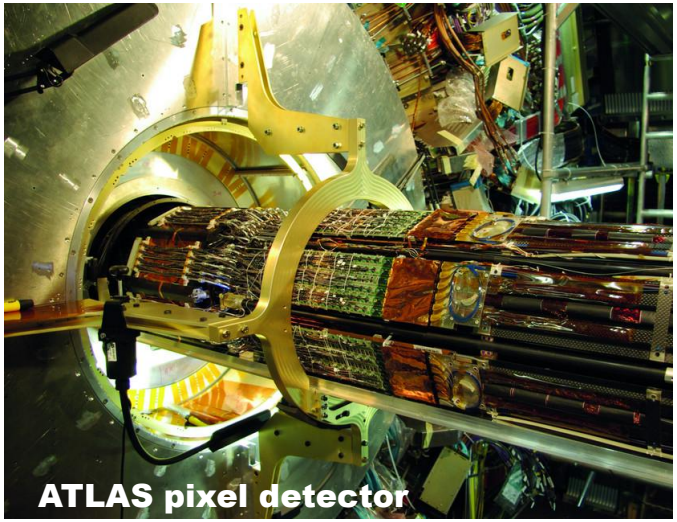
Moore's Law:"The number of transistors in a dense integrated circuit doubles every 18 months."

Si in HEP, a history of success too!



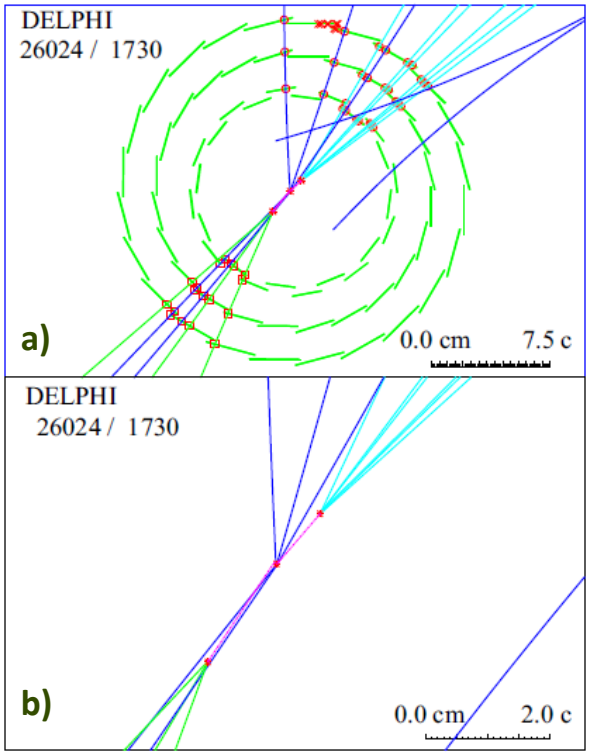






- Silicon detectors allows:
  - precise tracking and vertexing.
  - high precision momentum measurement.
  - detection of particles with very short lifetimes.
- Microelectronics:
  - large amount of data processing.
  - full custom electronics -> area and power reduction.
  - large scale -> lower cost.

Pixels for HEP detectors

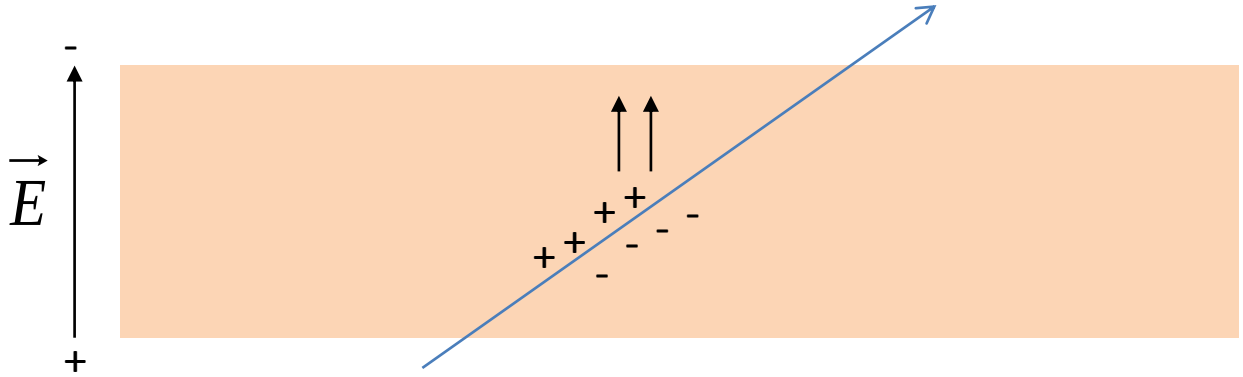


A b-event with the DELPHI vertex detector. a)track points of the three detector planes. b) event reconstruction. **[from CERN]**

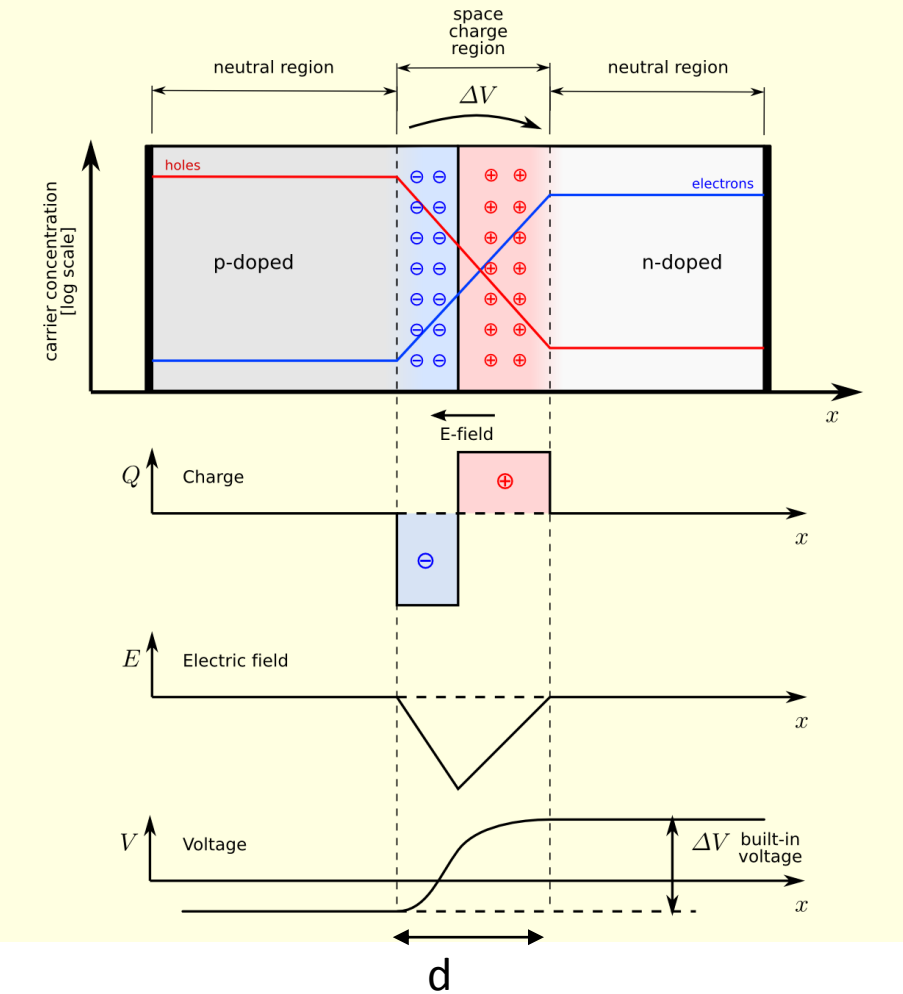
- Silicon detectors critical to reconstruct the path of the outgoing particles
- Some particles are unstable and decay before arriving to the detector, but with very precise (pixel) detectors their presence can be inferred
- Silicon detectors played a crucial role in new discoveries (eg, top quark)
- Vertex detectors measure the direction of charged particle's track precisely enough to allow the location of particle's origin.

Si features for HEP

- Si offers precision, compactness, and speed.
- 3.6eV needed to generate a e^-/h^+ pair. (15eV for argon).
- High ionization density: MIP creates 800.000 e^-/h per cm in Si but only 100 e^-/h per cm in a gas like argon.
- Number of free carriers (~10^9) >> generated number of electrons by ionization (~$2x10^4$) ➔ the sensor needs to be depleted from free carriers ➔ **PN junction**



PN junction (diode)

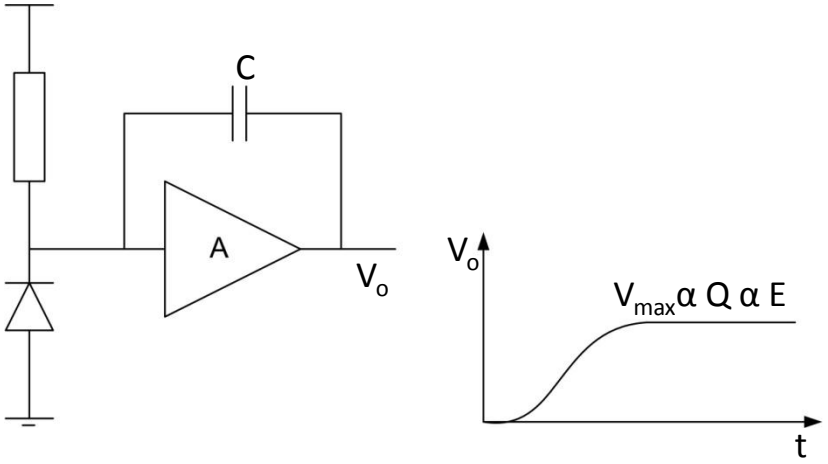


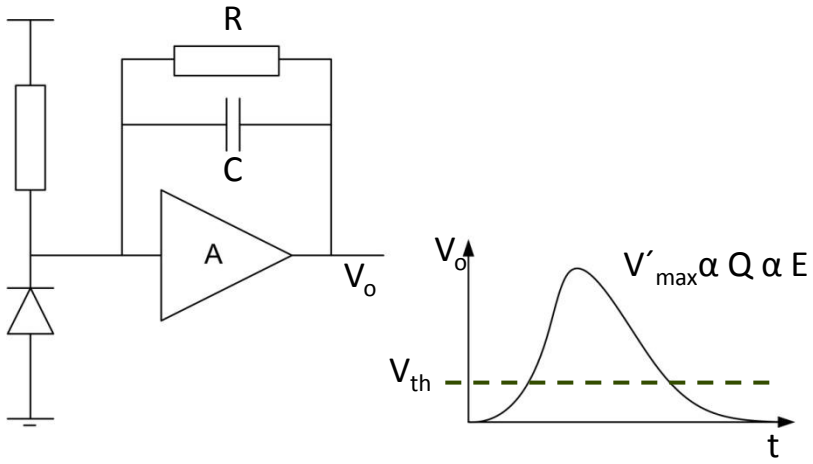
- At the interface of an n-type and p-type semiconductor there is a diffusion of surplus carries to the other material until thermal equilibrium is reached. The remaining ions create a space charge and an electric field stopping further diffusion.
- The stable space charge region is free of charge carries and is called the **depletion zone.**
- e^-/h pairs created at the depleted regions are swept by the electric field.
- Charge mainly collected by drift and not diffusion.
- Depletion region depth:

$$d = \sqrt{2 \cdot \varepsilon \cdot \rho \cdot V_{FD}}$$

- Total amount of generated charge is proportional to the depletion region!

Readout electronics





- Charge stored into the capacitor.
- Voltage is proportional to stored charge and hence to energy.
- To detect another hit the capacitor has to be reset. R introduces a discharging path.
- In some cases energy is not needed, only to if there has been a hit or not -> discriminator connected at the output of the charge sense amplifier.

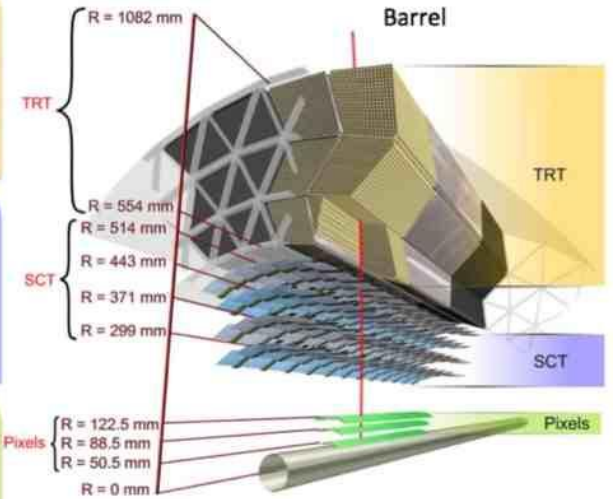
Pixel detectors

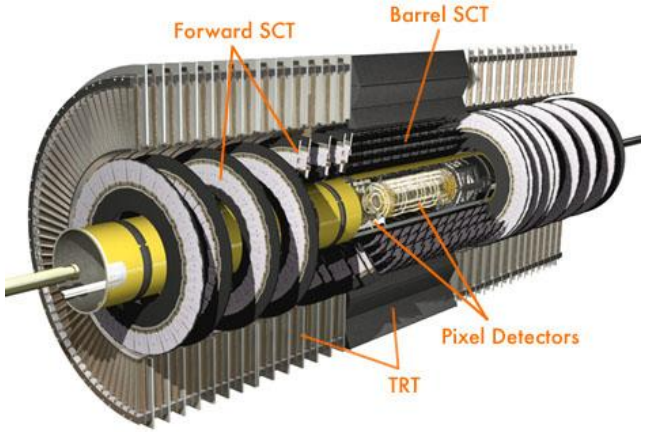
Silicon detectors on ATLAS

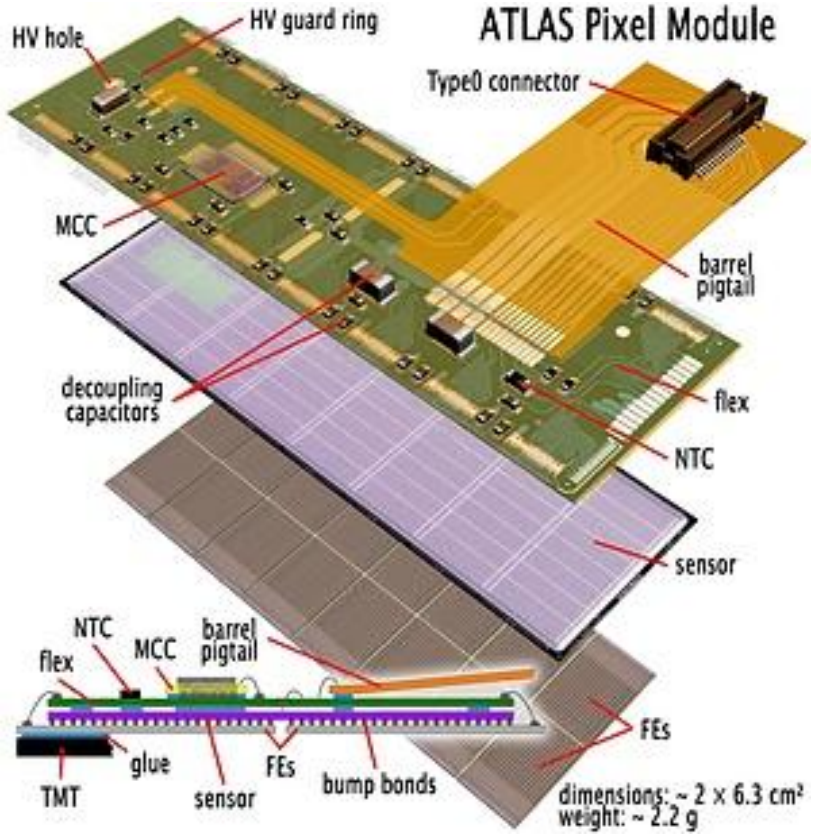
- Straw tracker + Transition Radiation
- 4mm diameter straws with 35 μm anode wire
- Layers: 73 in Barrel (axial) 2x160 in Endcap (radial)

- 4(9) double layers in Barrel/Endcap
- 4088 modules, 6M chan., strips 80 μm
- Resolution 17 x 580 μm

- 3 layers in Barrel and Endcap
- Pixel size 50 x 400 μm
- Resolution 10 x110 μm
- 80 M channels

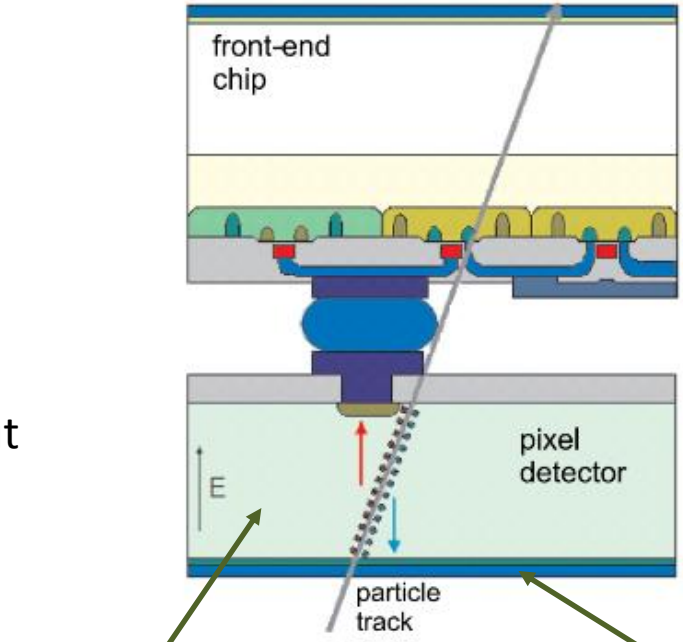


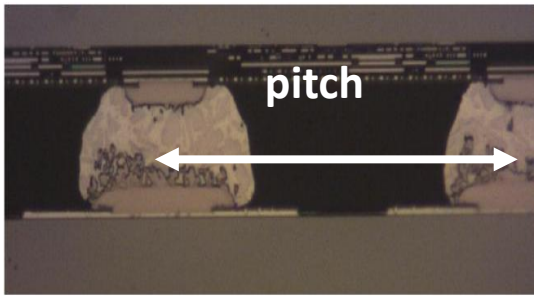


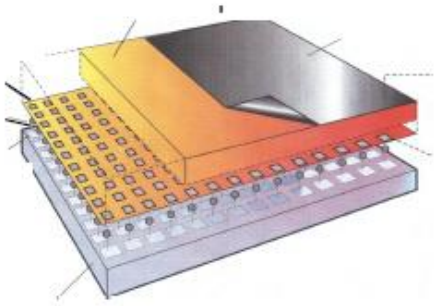


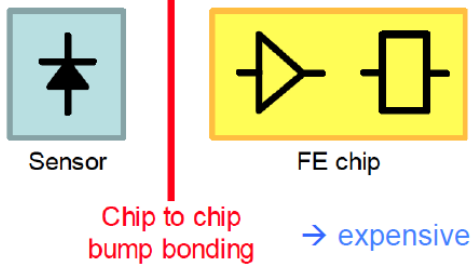
Pixels for HEP detectors

- **Hybrid pixels:**
  - -fully depleted sensor
  - -expensive high quality substrate
  - -backside processing
  - -high resistivity
  - -thickness ~250µm
  - -charge collection by drift
- Optimum technologies for sensor and readout chips.
- Assembly by bump bonding.
- Expensive hibridization process.



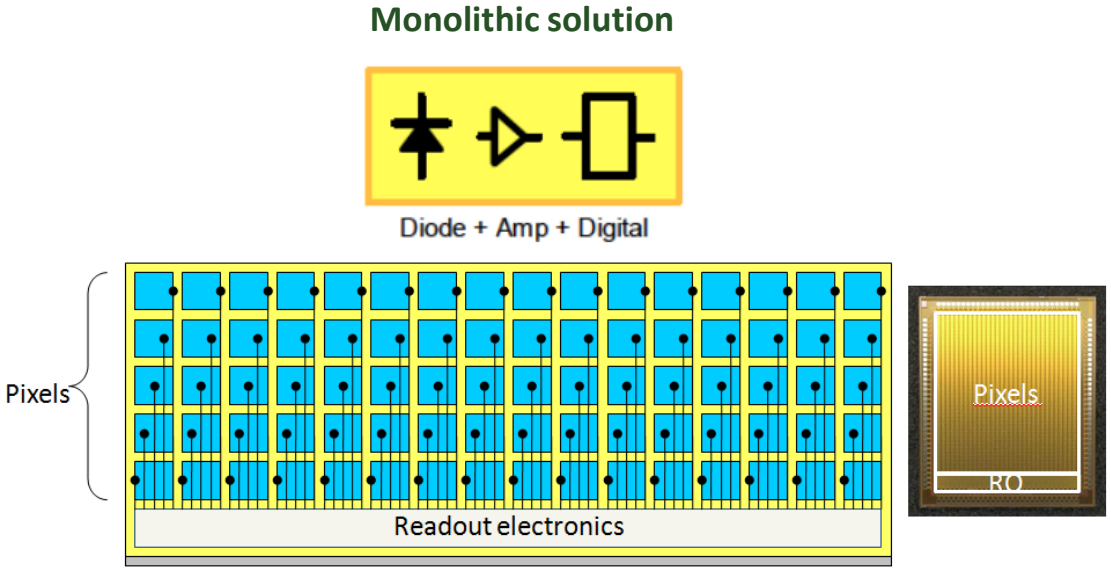






Pixels for HEP detectors

- **Depleted Monolithic Active Pixels (DMAPS)** based on standard CMOS technologies.
- Large scale and low cost.
- Pixels and readout electronics on the same chip (fully monolithic detector).
- Thinner detectors.

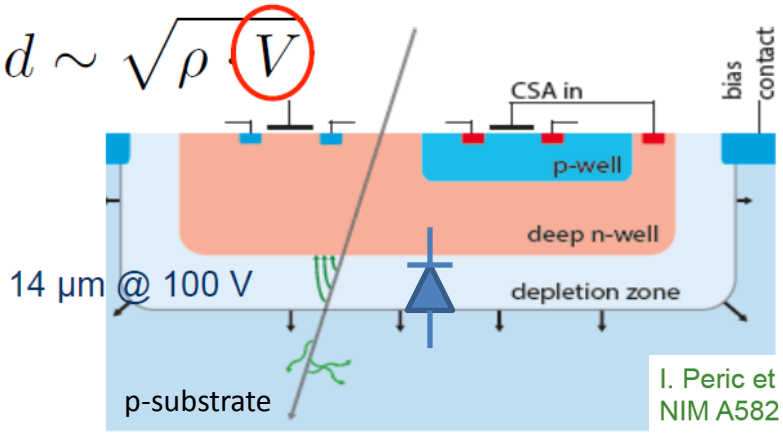


DMAPS

- Charge collection by drift and fast (<10ns).
- Ideal Depleted MAPS (DMAPS):
  - High resistivity silicon substrate.
  - Biased at High Voltage.
  - PMOS and NMOS based circuits.
  - Backside contact.

$$d \propto \sqrt{\rho . V}$$

High Voltage MAPS (HV-MAPS)



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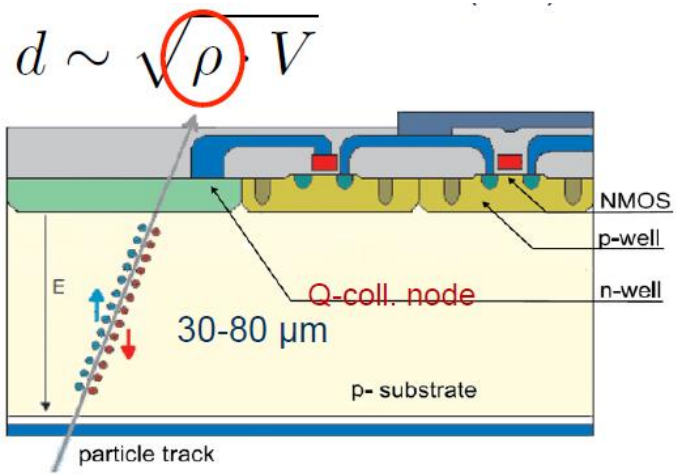
High Resistivity MAPS (HR-MAPS)



R&D program

- **Challenges for HL-LHC:**

	Inner layers (<6cm)	Outer layers (>25cm)
High rates	10 MHz/mm^2	1 MHz/mm^2
Radiation	> 1 Grad TID 2x10^{16}n$_{eq}$/cm^2	> 50 Mrad TID 1x10^{15}n$_{eq}$/cm^2

- Experimental results from various vendors show good radiation hardness efficiency, and substantial depletion depth.
- A lot of R&D is still pending to validate this technology for ATLAS inner tracker upgrade.:
  - Multi-project wafers chips submitted to many foundries to evaluate feasibility.
  - Irradiation campaigns to evaluate radiation hardness.
  - Lab and test beam characterization to evaluate detection efficiency and tracking properties.

R&D program

KIT, IFAE, Liverpool, UCLA	Bonn, KIT, SLAC	Bonn	Bonn, Prague
AMS	**LFoundry**	**XFAB**	**ESPROS**
• High-Voltage process with module up to 120V • Possibility to use high-resistivity p-type wafers (experimental) • CMOS 350nm and 180nm available • No full CMOS insulation • No backside processing	• High-Voltage process • High-resistivity p-type wafers part of standard process • CMOS 150 nm available • Full CMOS insulation • No backside processing	• SOI 150nm CMOS process • 1.8/5V modules • 100 Ohm*cm standard wafer material, possibility to go up to 1 kOhm*cm • No backside biasing • Sensor and CMOS volumes decoupled (SOI)	• 150nm CMOS process with 14V module • High-resistivity , 50um thin n-type wafers used a standard processing material • Full CMOS isolation • Backside processing part of the standard process

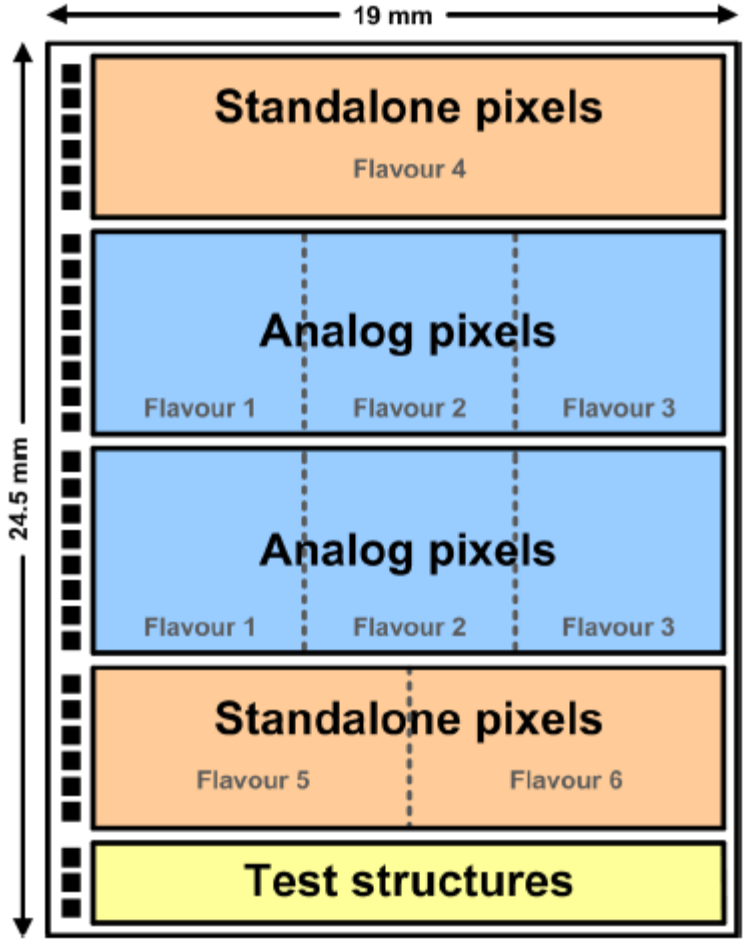
From M. Benoit

- More advanced R&D program
- **Mu3e experiment will include HV-MAPS.**

H35 demonstrator

H35 demonstrator

Floorplan



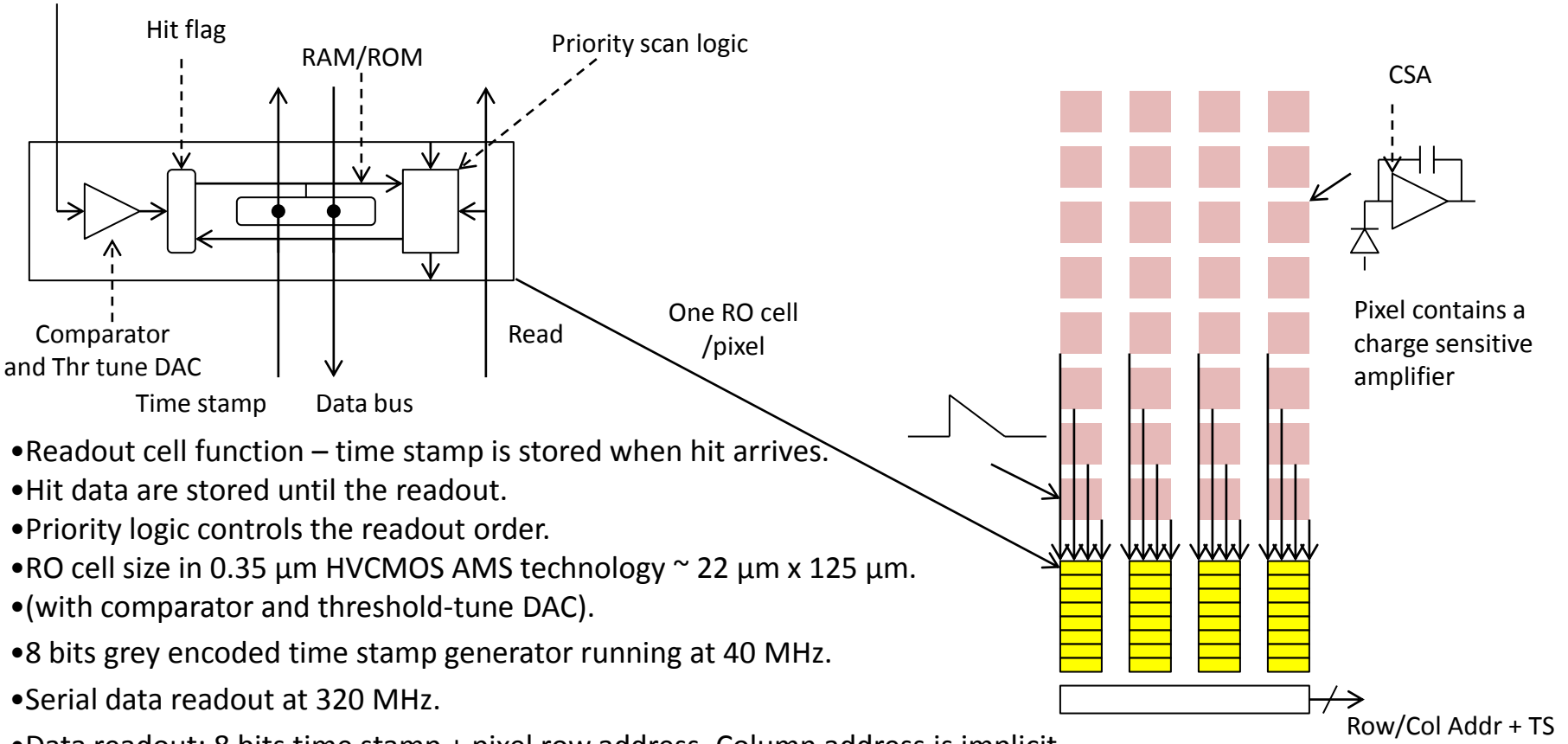
Main features:

- AMS 0.35µm HV CMOS technology.
- submission through an engineering run.
- different substrate resistivity: 20Ω·cm, 200 Ω·cm, 1000 Ω·cm.
- analog pixels with FEI4 coupling for readout.
- digital pixels with standalone digital readout.
- test structures (diodes and extra pixels).
- pixel size: 250 µm x 50 µm.

From E. Vilella

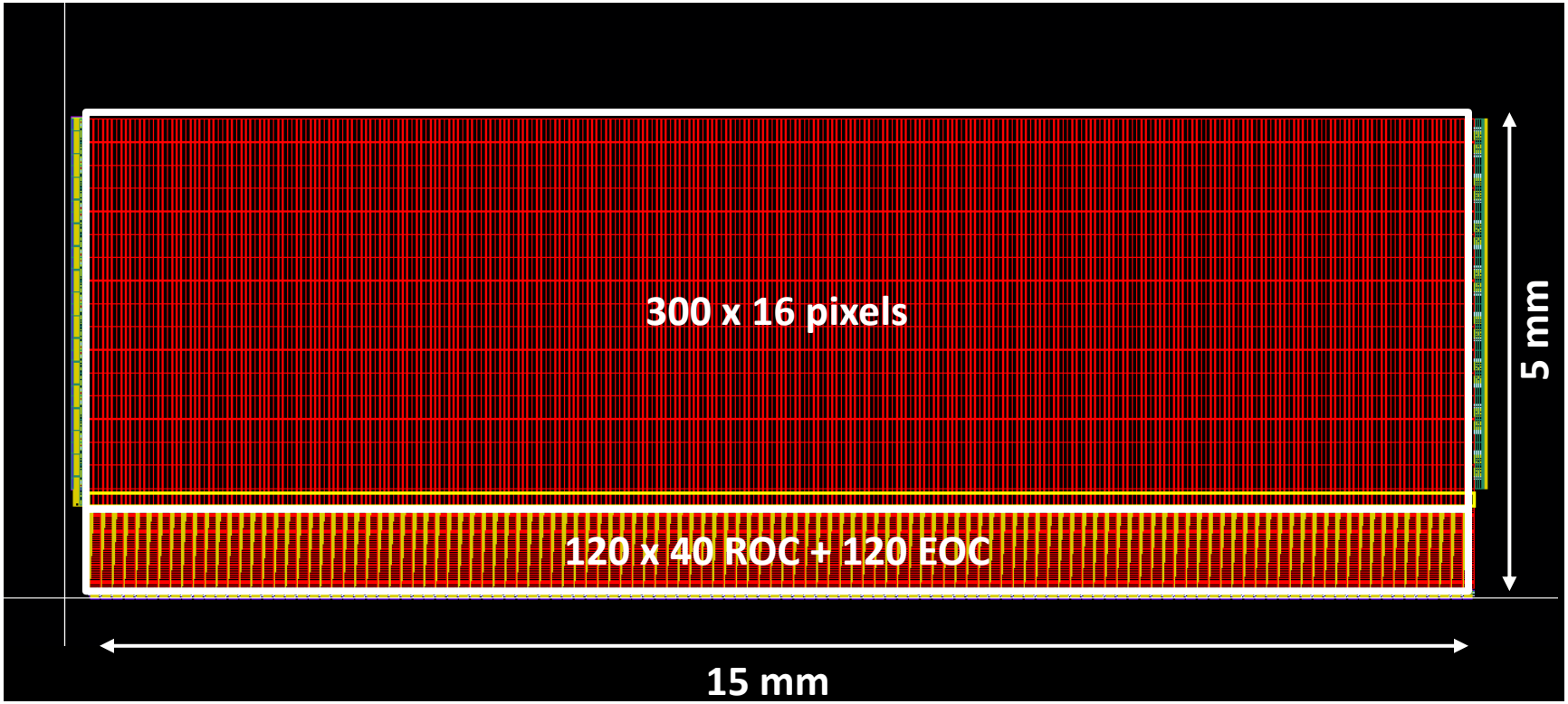
Standalone pixels

Concept: Every pixel has its own readout cell, placed on the chip periphery



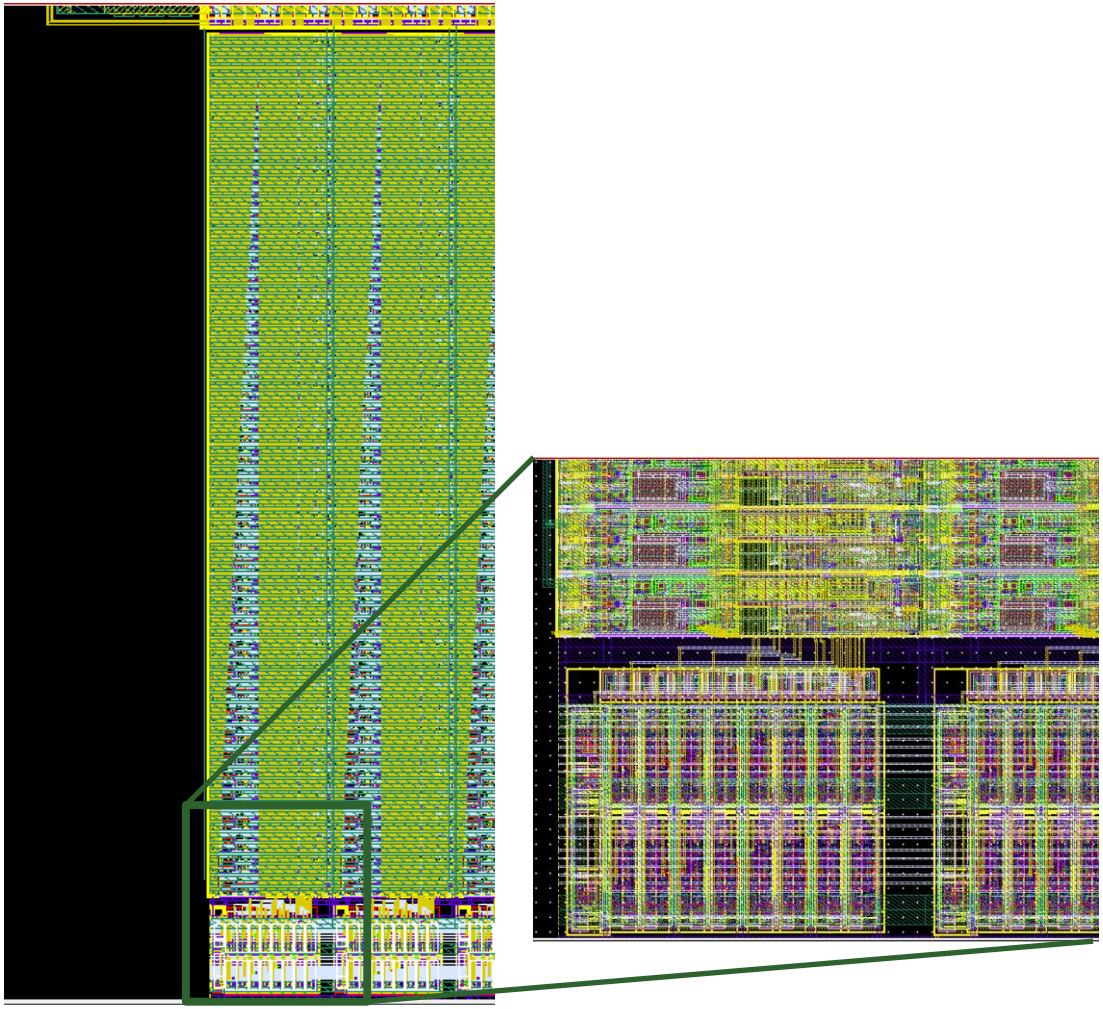
- Readout cell function – time stamp is stored when hit arrives.
- Hit data are stored until the readout.
- Priority logic controls the readout order.
- RO cell size in 0.35 µm HVCMOS AMS technology ~ 22 µm x 125 µm.
- (with comparator and threshold-tune DAC).
- 8 bits grey encoded time stamp generator running at 40 MHz.
- Serial data readout at 320 MHz.
- Data readout: 8 bits time stamp + pixel row address. Column address is implicit.
- Pixels read at 40MHz, one at a time.
- Read time of a 60 column row: 1.5µs.

Standalone pixels layout

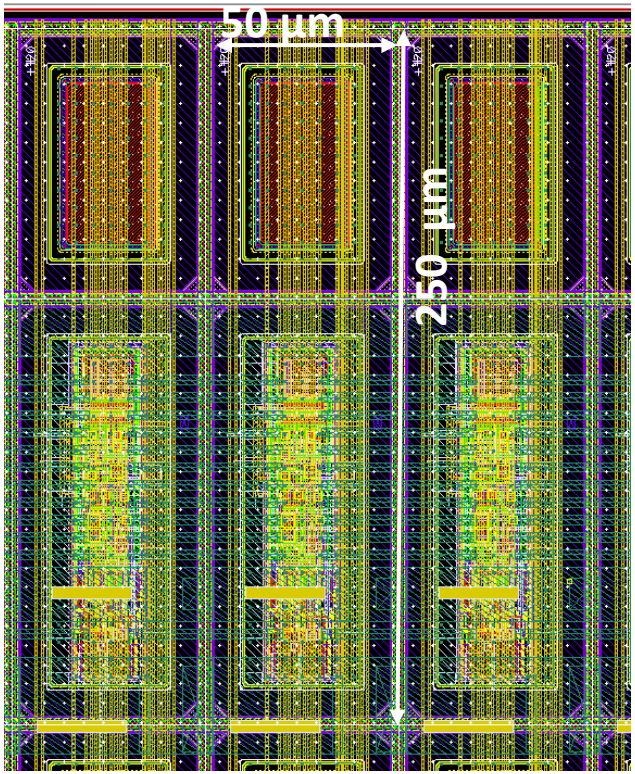


Standalone pixels layout

Readout columns



Pixels



Conclusions

- Hybrid pixel detectors have proved very successful but they are expensive. Sensor and readout electronics on separated devices ->optimum technologies are used.
- DMAPS, cheaper solution due to the use of standard CMOS technologies and the possibility of integrating the sensors and the readout electronics on the same chip.
- Exciting moment: a lot of R&D being carried out. Several institutes working on DMAPS.
- HL-LHC:
  - outer layers, may fit but still a lot of R&D to be done!
  - inner layers, probably not.
- DMAPS collaboration with KIT, University of Liverpool and University of Geneva:
  - A first prototype will be submitted in July and a second prototype will be submitted by then of the year.
  - Development of the DAQ.
- HVMAPS not only for ATLAS, other potential applications.

Thank you for your attention!

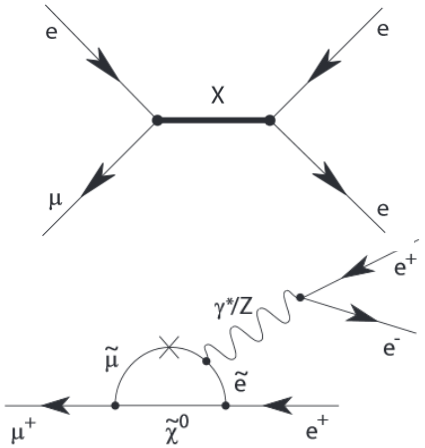
Mu3e experiment

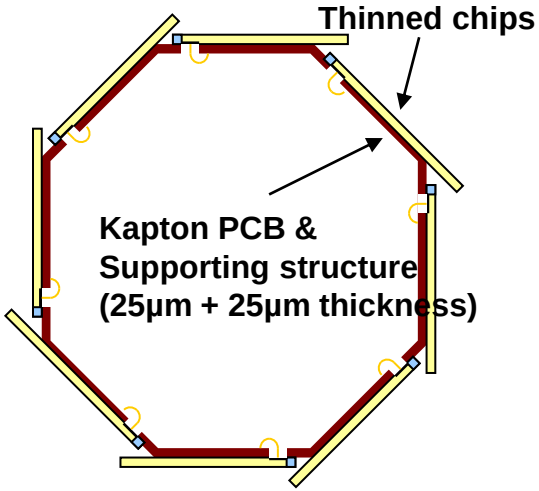
- Search for decay $\mu^+ \rightarrow e^+ e^- e^+$ with a BR sensitivity < 10^{-16} (4 orders of magnitude better than previous searches).
- Several background sources, the most important is the decay:

$$\mu^+ \rightarrow e^+ e^- e^+ \bar{\nu}_\mu \nu_e$$

which is indistinguishable from signal except for the missing momentum carried away by the neutrinos. **It can only by suppressed via a very precise momentum measurement** :

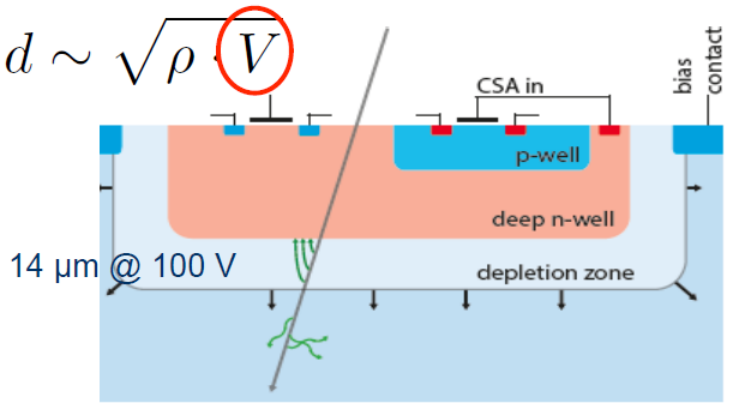
-Low Coulomb scattering -> very thin sensors

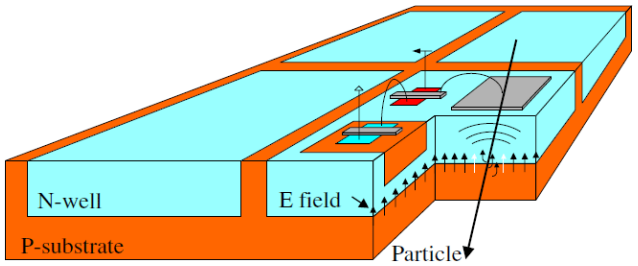




HV-MAPS

- HVCMOS detectors are depleted active segmented detectors implemented in a CMOS process.
- The electronics is placed inside the n-well sensor electrode.
- High voltage is used to deplete a part of the substrate.
- The main charge collection mechanism is drift of the charge signal from the depleted region.
- HVCMOS can be implemented in standard CMOS technologies
- These technologies have substrate resistances of 10 to 20 Ωcm.
- The HVCMOS structure can be improved by taking a substrate of higher resistance (for instance 100 – 1000 Ωcm) instead of the standard one. (Non-standard CMOS process).





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