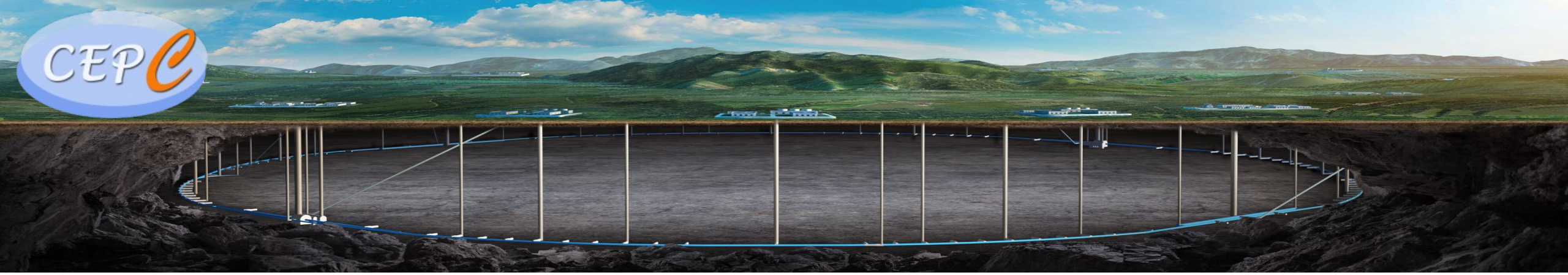


CEPC vertex Detector

Zhijun Liang
(On behalf of the CEPC physics and detector group)

2025 European Edition of the International Workshop on the Circular Electron-Positron Collider (CEPC), Barcelona, Spain

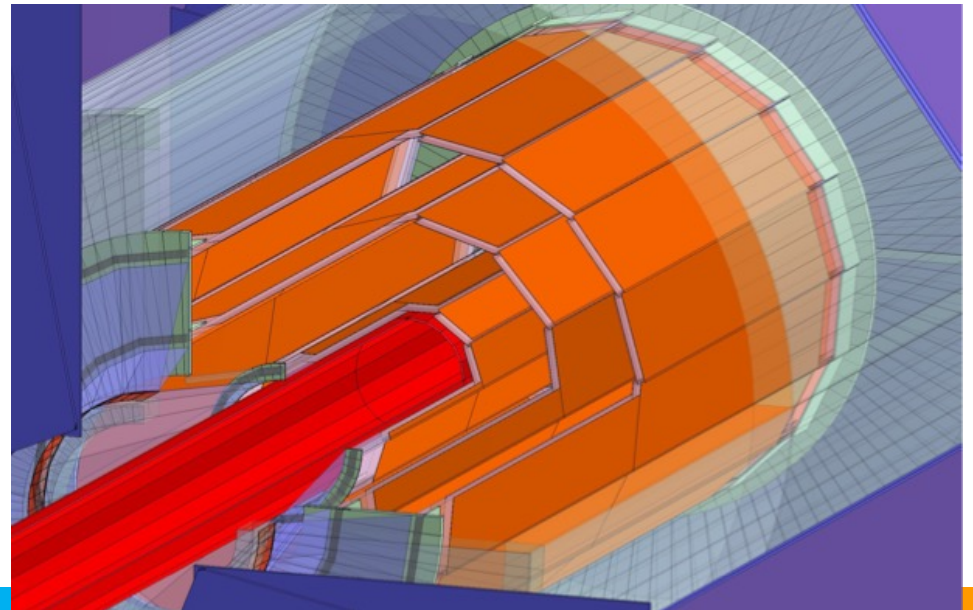
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

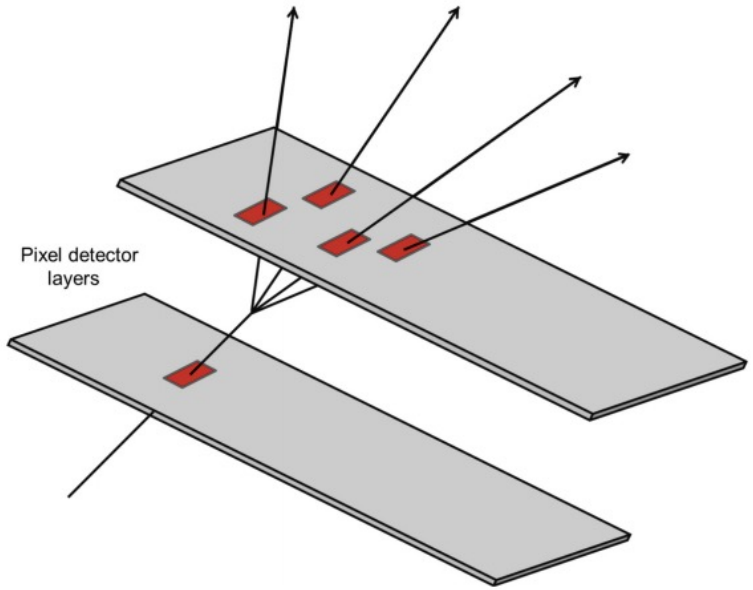
Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics & BEC
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z)
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC





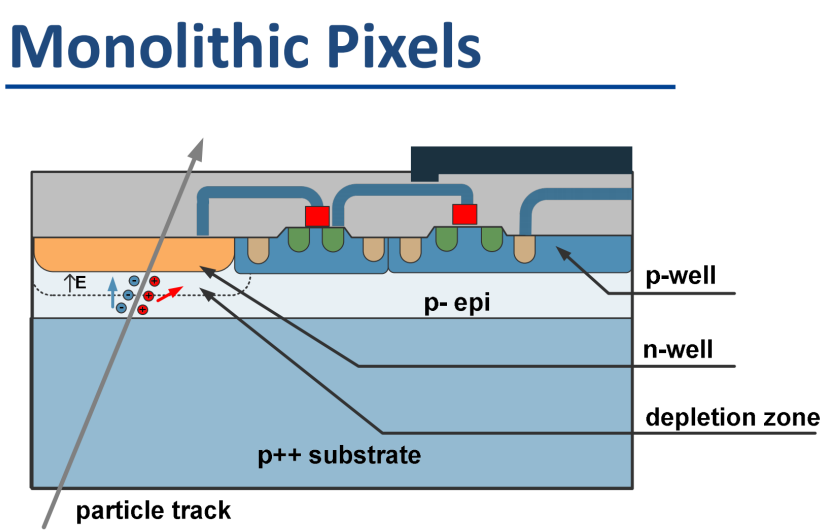
Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)
- High data rate: (especially at Z pole , ~43MHz, 1Gbps per chip)
  - **Challenges**: 1Gbps per chip high data rate especially at Z pole
- Low material budget (less than 0.15%X0 per layer)
- Detector Cooling with air cooling (power consumption<=40 mW/cm^2)
- Spatial Resolution (3-5 um)
- Radiation level (~1Mrad per year in average)

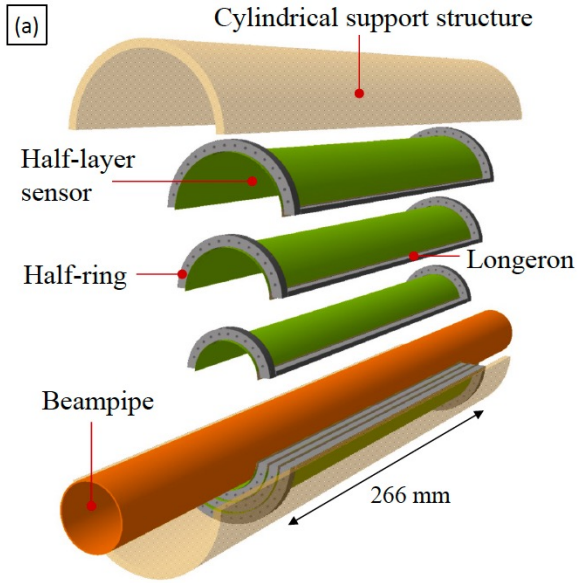
Technology for CEPC Reference TDR

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

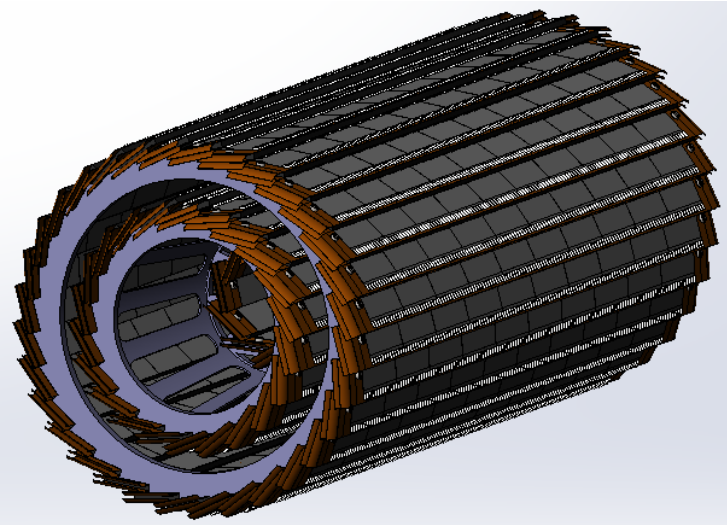
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11×11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

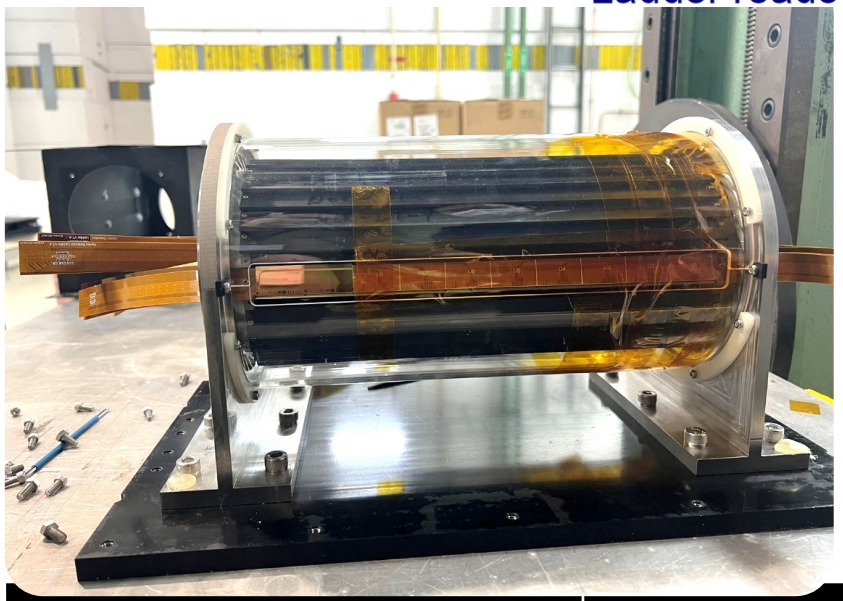
R&D effort: vertex detector prototype

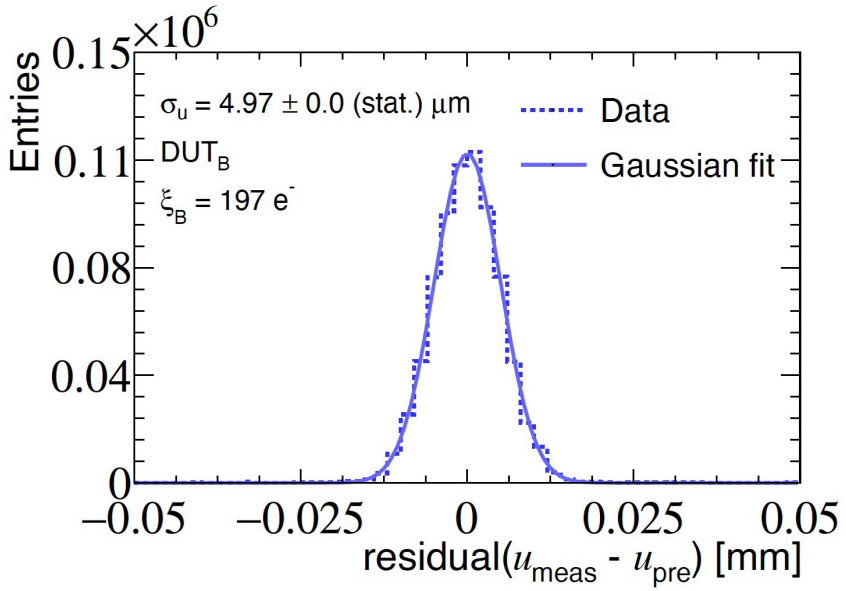
Collaboration with IFAE in TaichuPix development

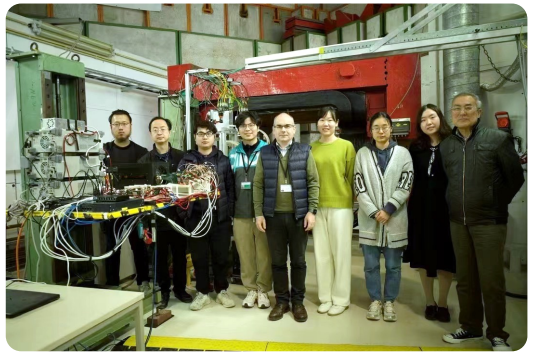
TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**

Ladder readout sy



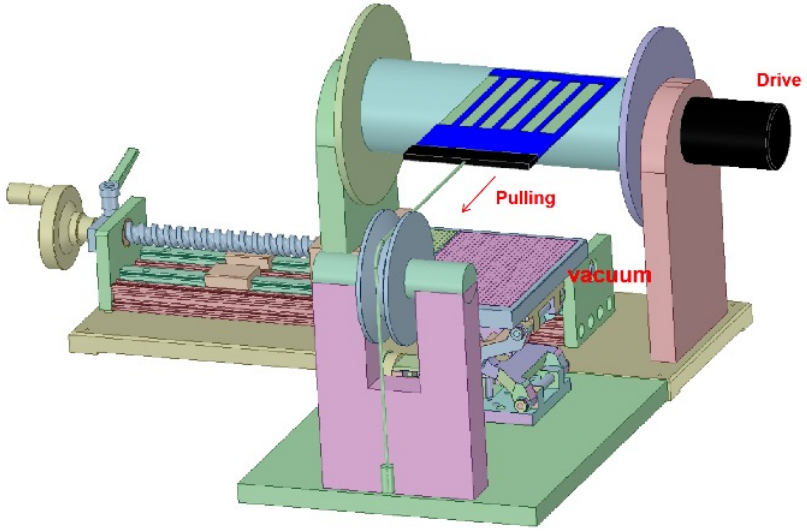


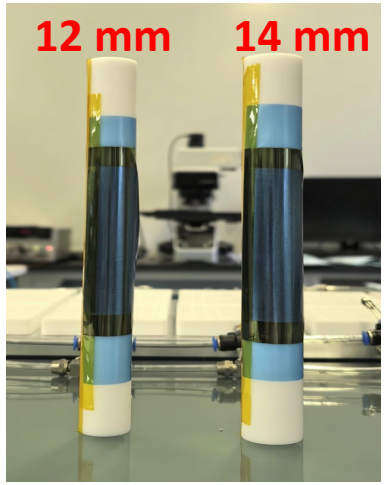


	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm





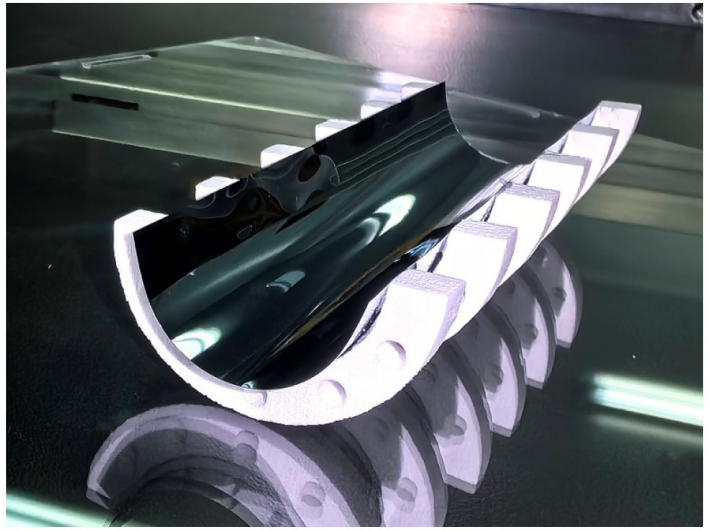
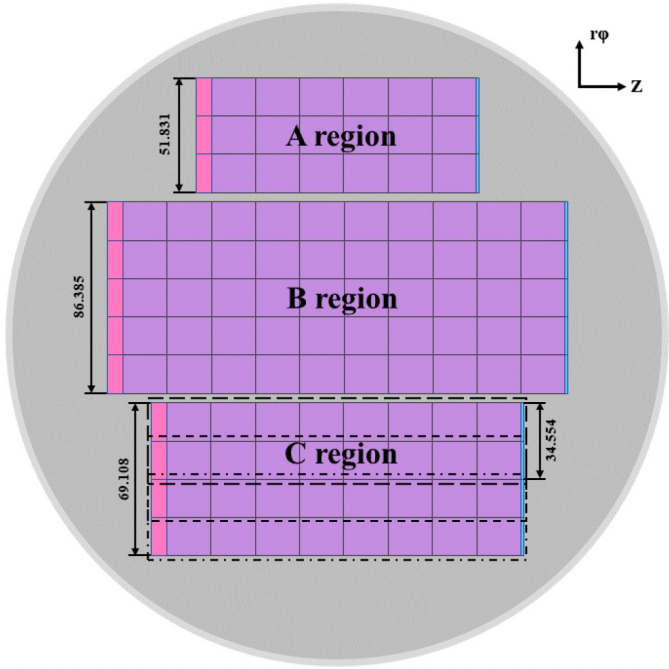


Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

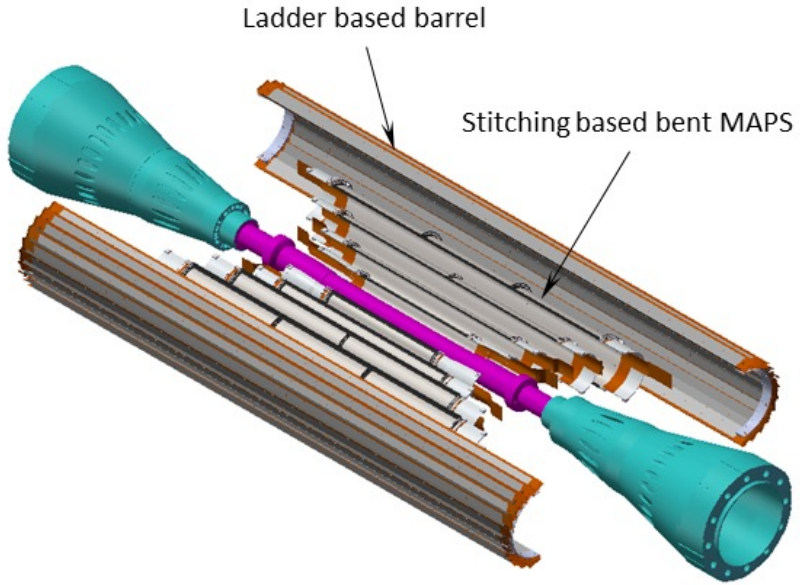
Baseline layout

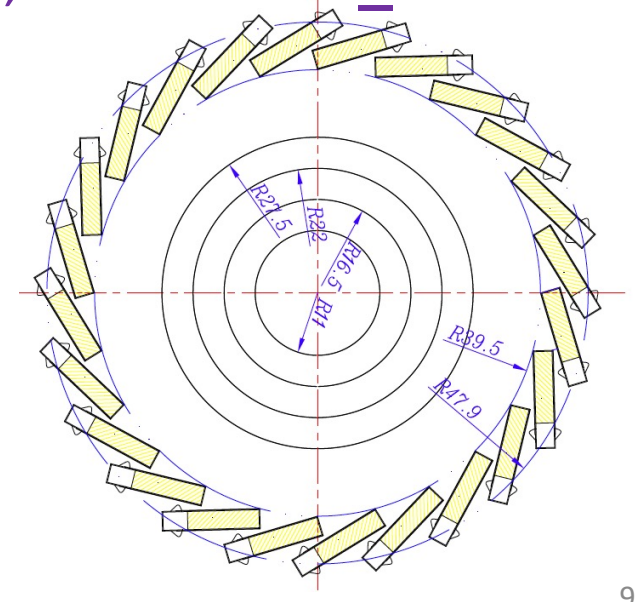
- Baseline :4 single layer of bent MAPS + 1 double layer ladders
  - Alternative option: 3 double layer ladders
- Inner layer: Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: Double layer Ladder (~0.3% X0 per layer)



Long barrel baseline layout (no endcap disk), to cover cos θ<=0.991

Layout	BVTX/ PVTX X	radius mm	length mm
Baseline	BVTX 1	11.1	161.4
	BVTX 2	16.6	242.2
	BVTX 3	22.1	323.0
	BVTX 4	27.6	403.8
	PVTX 5-6	39.5	682.0





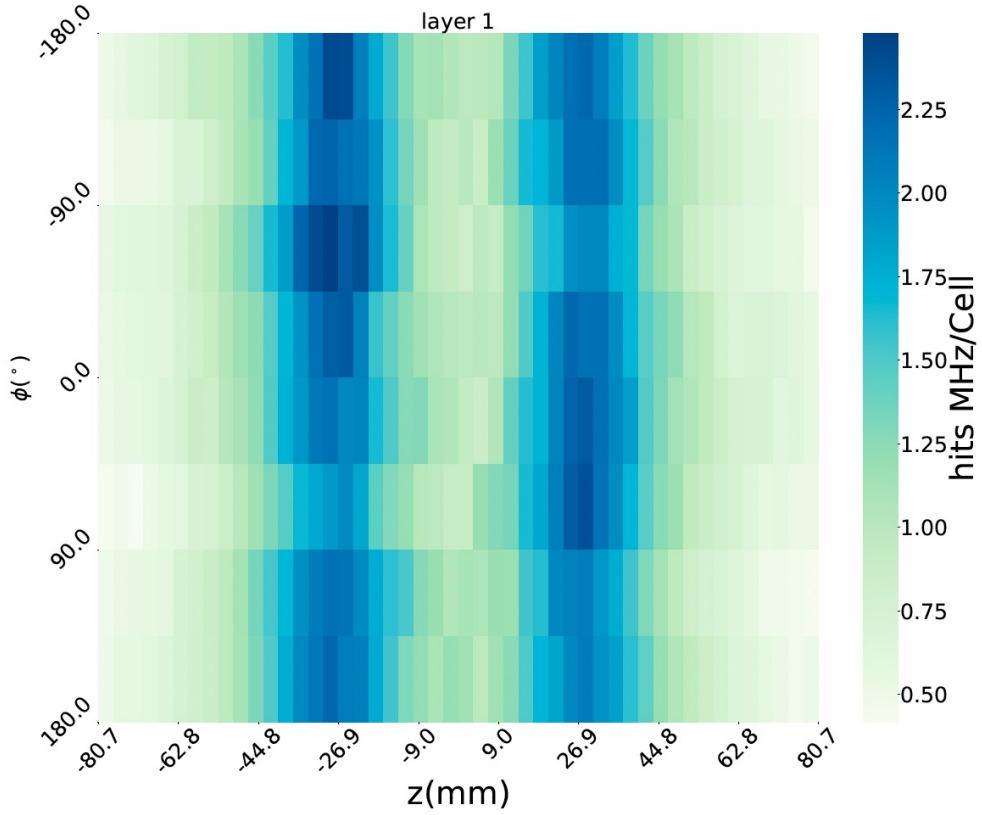
Background estimatoin

- Background rate are simulated
  - The data rate at low-lumi Z pole is about ~Gbps level in b-layer.

Background rate for Higgs and low-lumi Z runs

Layer	Ave. Hit Rate MHz/cm^2	Max. Hit Rate MHz/cm^2	Ave. Hit Rate×C MHz/cm^2	Max. Hit Rate×C MHz/cm^2	Ave. Data Rate Mbps/cm^2	Max. Data Rate Mbps/cm^2
Higgs: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 346ns, 53 %Gap, 25× 25 μm^2/ pixel)						
1	2.45	2.79	8.17	10.48	261.29	335.36
2	0.67	1.07	2.18	3.48	69.59	111.41
3	0.17	0.35	0.62	1.19	19.68	38.21
4	0.08	0.18	0.32	0.98	10.25	31.39
5	0.03	0.15	0.11	0.74	3.41	23.73
6	0.02	0.09	0.07	0.41	2.37	13.24
Zmode: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 69ns, 9 %Gap, 25× 25 μm^2/ pixel)						
1	9.35	18.68	42.45	88.23	1358.33	2823.36
2	0.89	1.47	3.73	7.54	119.24	241.36
3	0.31	0.75	1.45	5.99	46.49	191.75
4	0.19	0.47	0.95	4.86	30.50	155.50
5	0.05	0.10	0.20	0.45	6.40	14.38
6	0.04	0.07	0.15	0.38	4.80	12.17

Hit rate map for 1st layer @ low-lumi Z run



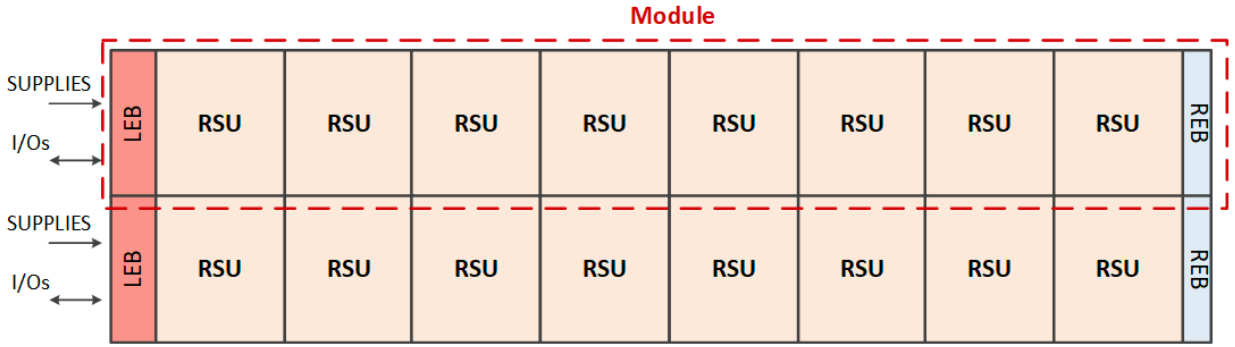
Electronics

– Baseline: Stitching

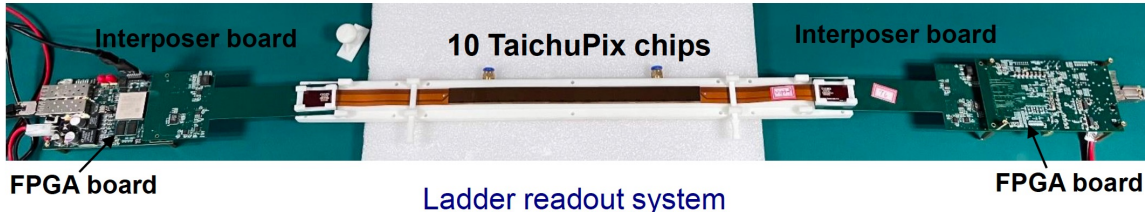
– Alternative: Flexible PCB (also used in layer 5/6)

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

Baseline: ALICE ITS3 like stitching

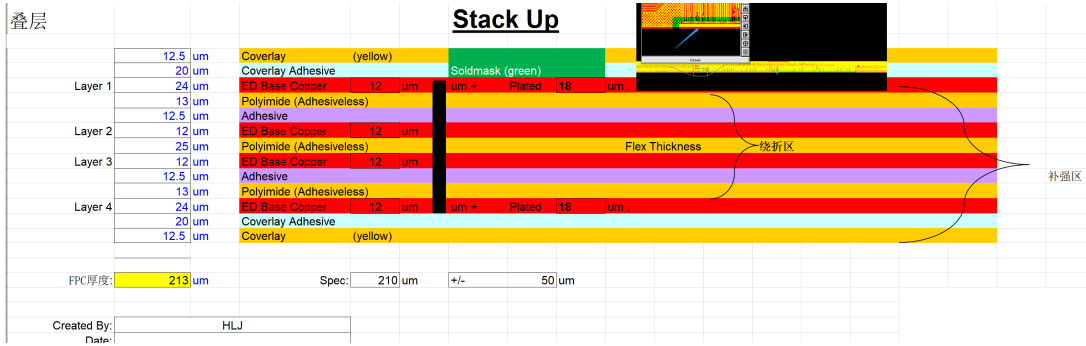


Alternative: flexible PCB



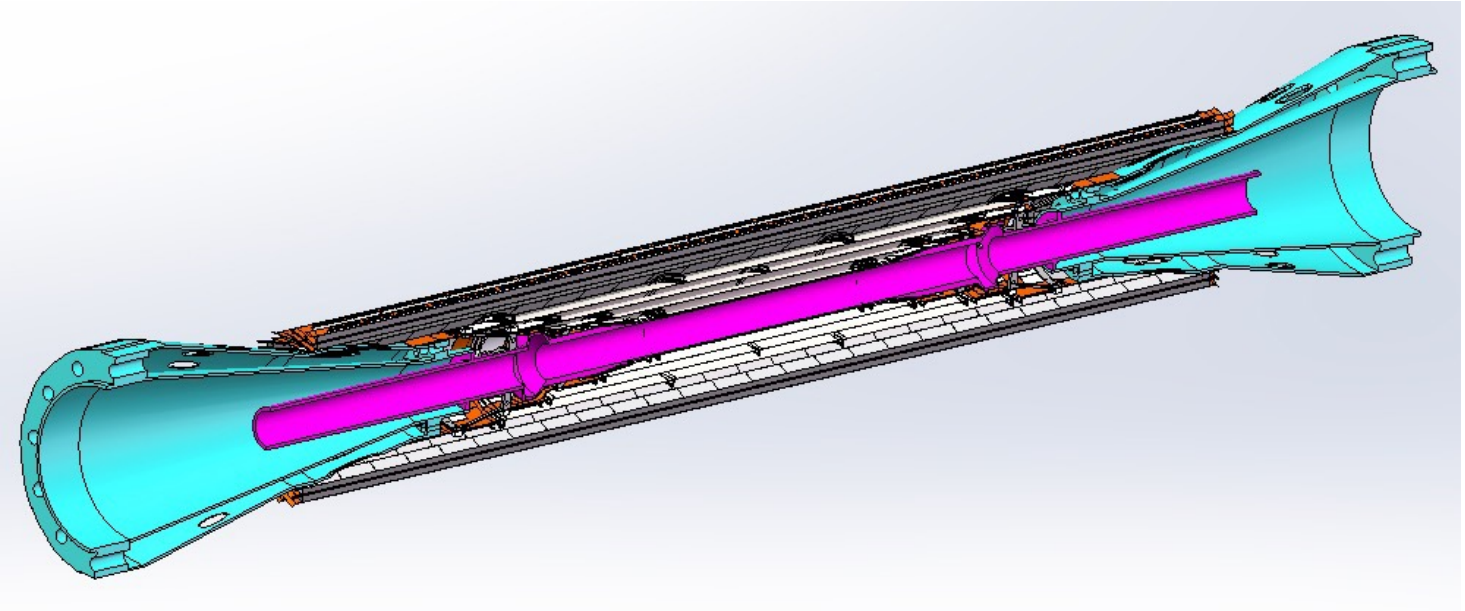
Estimates of average power dissipation per unit area

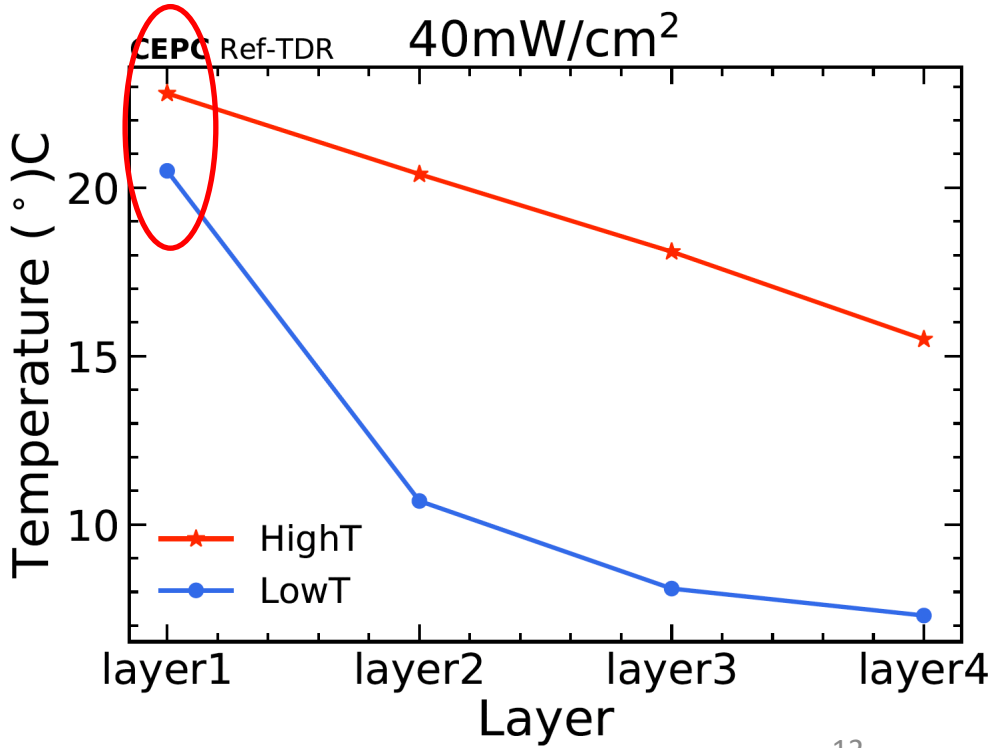
Components	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-End Block	485



Mechanics and cooling

- Benefitted from 65nm technology, Power consumption at low lumi Z can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down below 30 ℃ with 3.5m/s air speed for stitching layers





Alignment in stitching layer

- Deformation mode simulated by FEA.

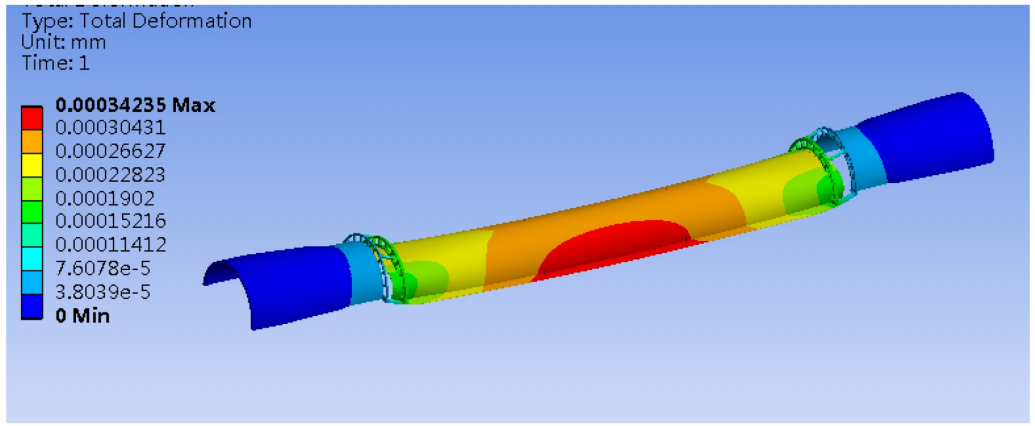
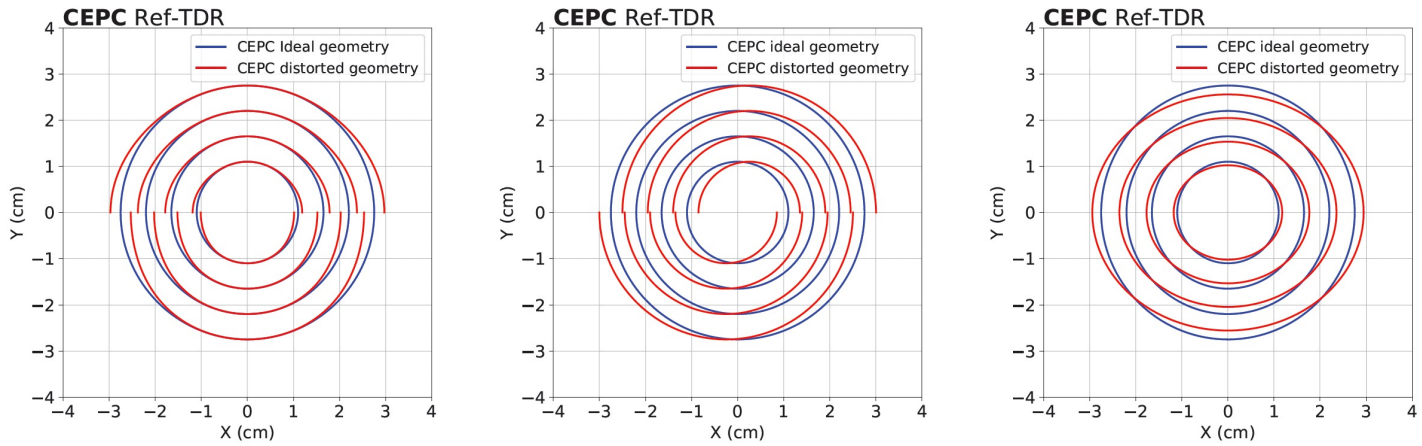
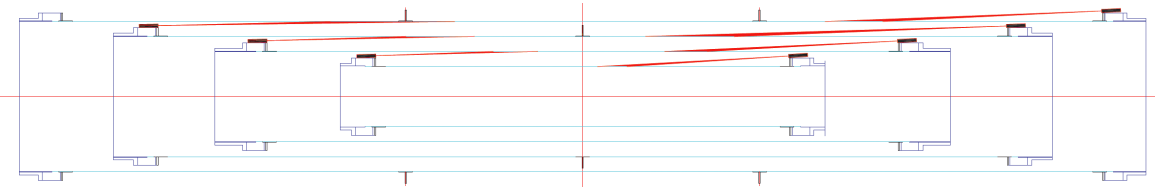


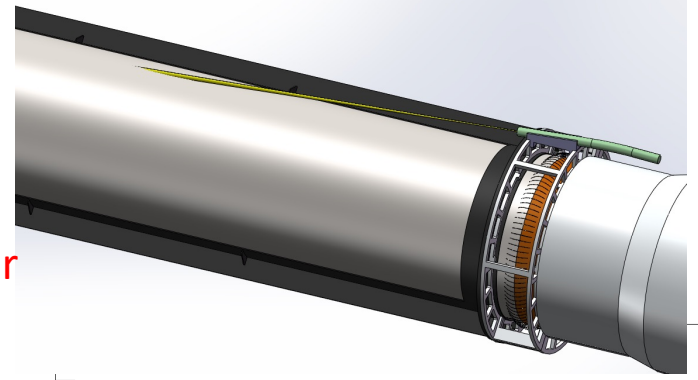
Figure 4.71: The simulated defromation of the inner layer bent MAPS half cylinder.



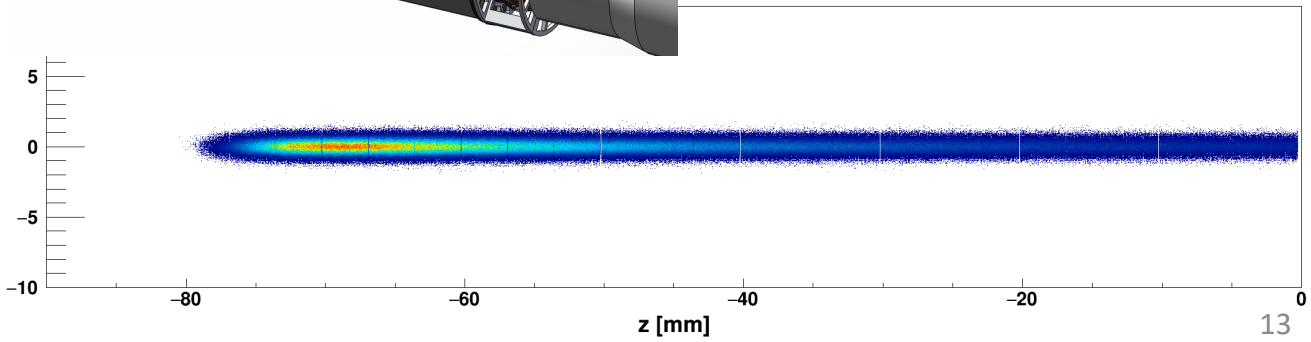
- Real time Deformation monitoring by infra-red laser alignment system

2D and 3D model on laser alignment system on vertex detector (inspired by CMS tracker laser alignment)



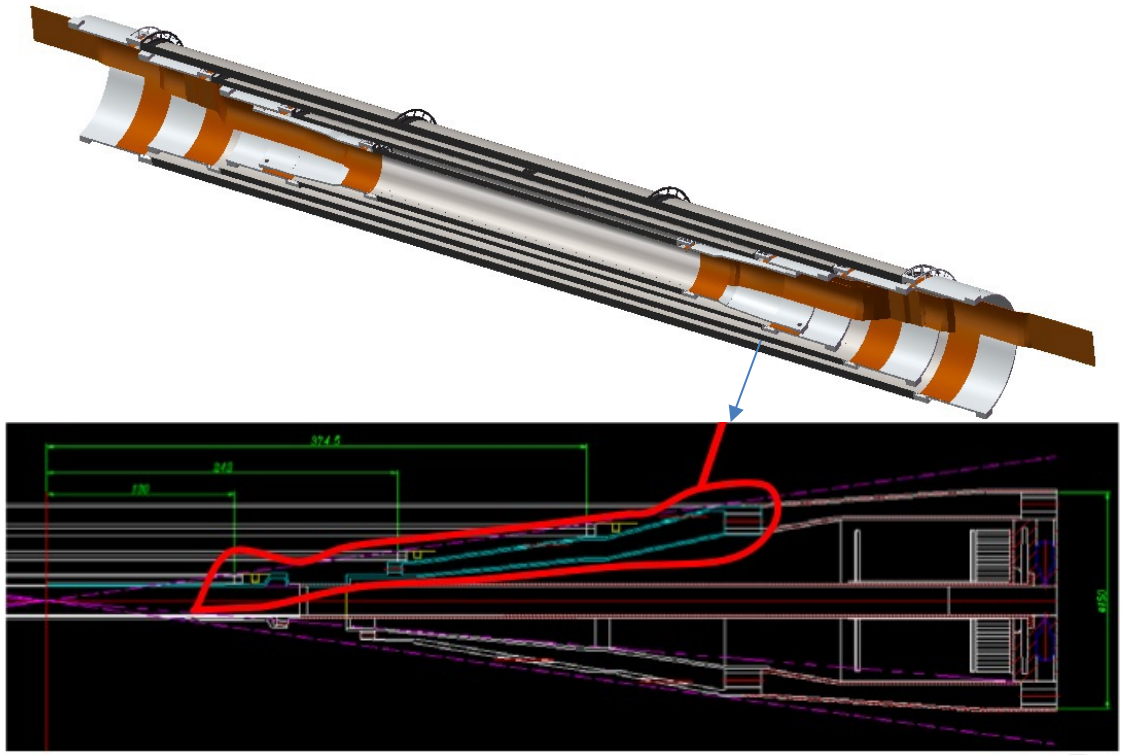


laser beamspot on bent-MAPS

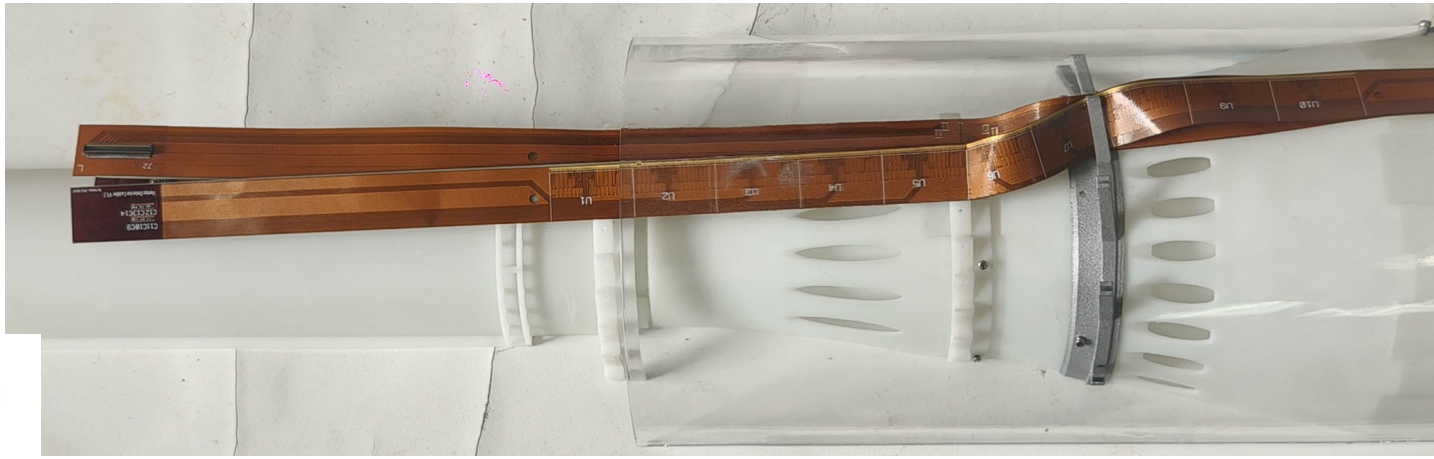


Vertex technologies: Cables and services

- Limited space in the MDI region for cables and services
  - Signal are transmitted by a flexible PCB then converted to fiber out of MDI region
  - Feasibility study with 3D printing mockup



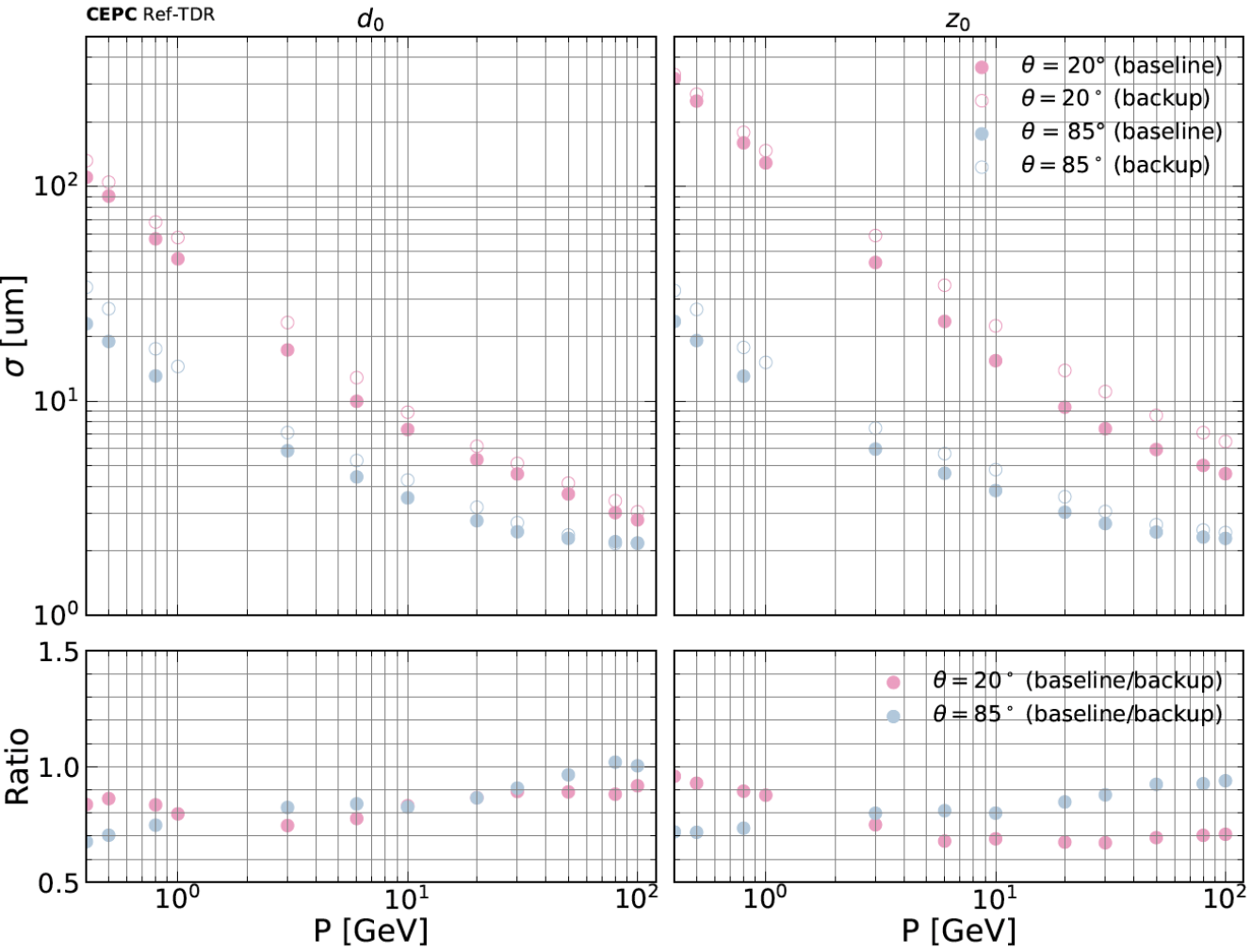
Cables routing using 3D printed model



Performance: impact parameter resolution

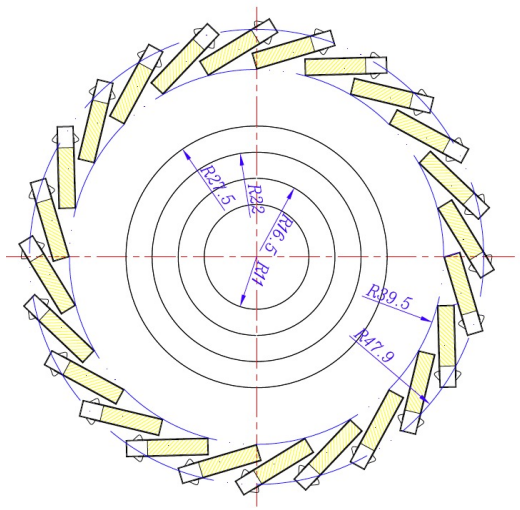
- Baseline has better resolution than alternative (ladder) (25-40%) in low momentum

d0 resolution: Baseline Vs backup layout

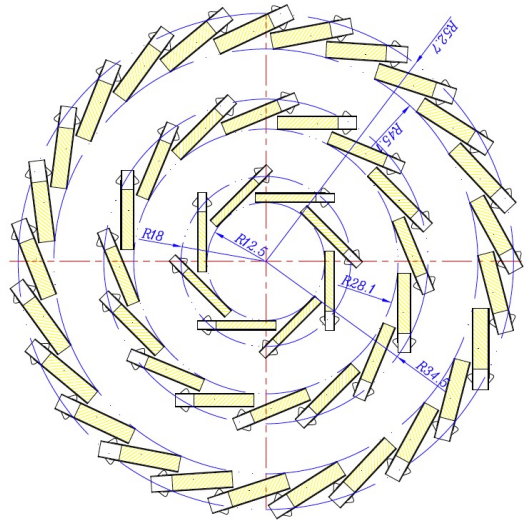


30%

Baseline layer
4 stitching +
1 double layer ladders

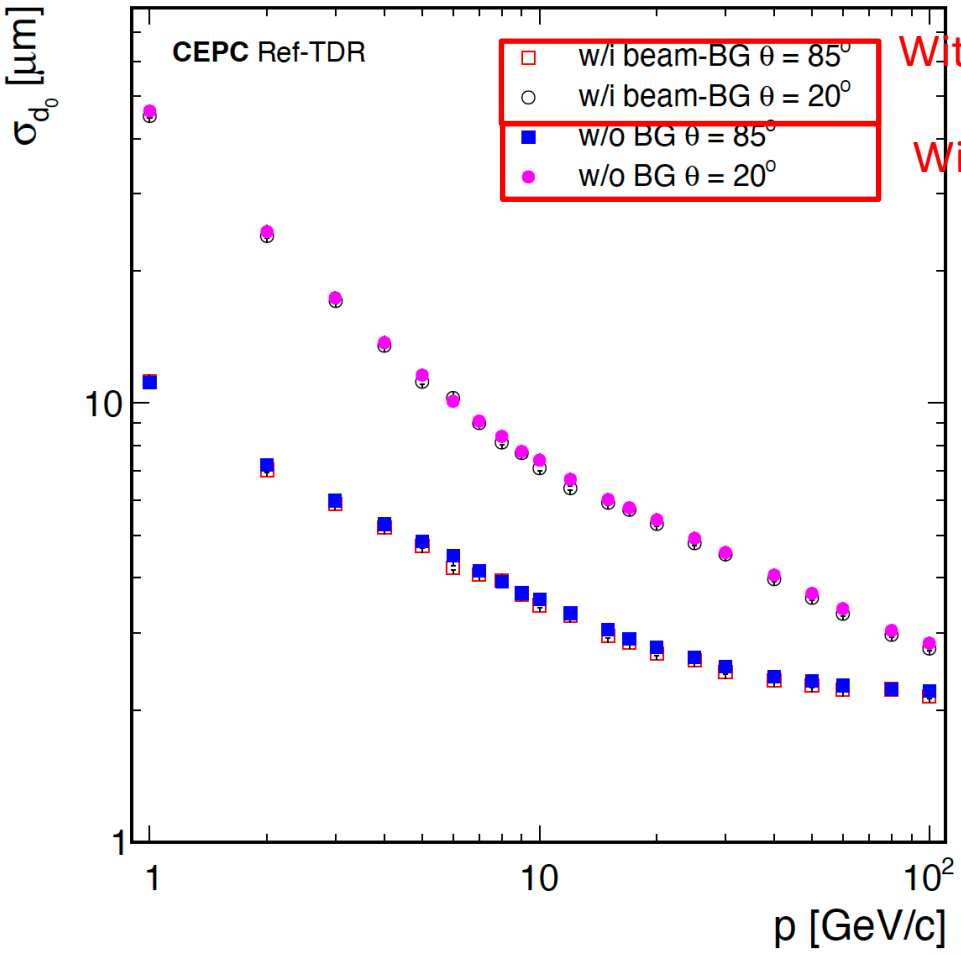


Backup layout
3 double layer ladders



Performance: Impact of beam background

- Overlay physics events with simulated beam background
  - No visible difference in performance w/wo background, computing time increased

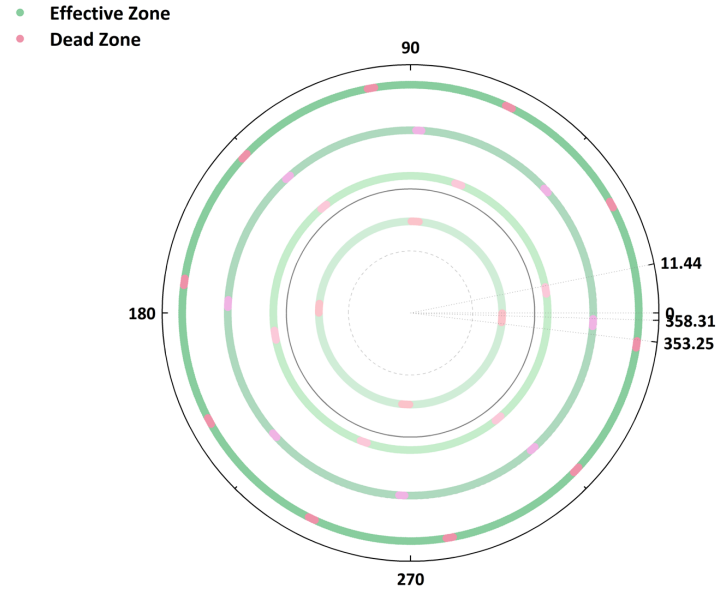


With beam background hits

Without beam background hits

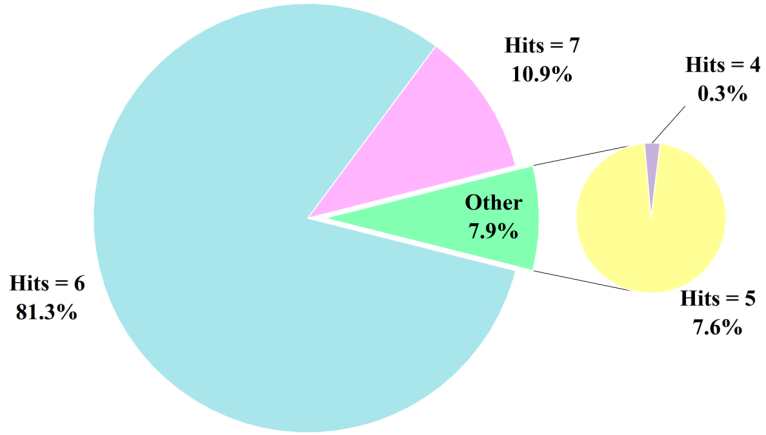
Performance: Efficiency

- A few percent Inefficiency expected in stitching layer
- Sensor (RSU) has inefficiency region in power stitch
- 99.7% of the track with >=4 hits (6 hits expected)

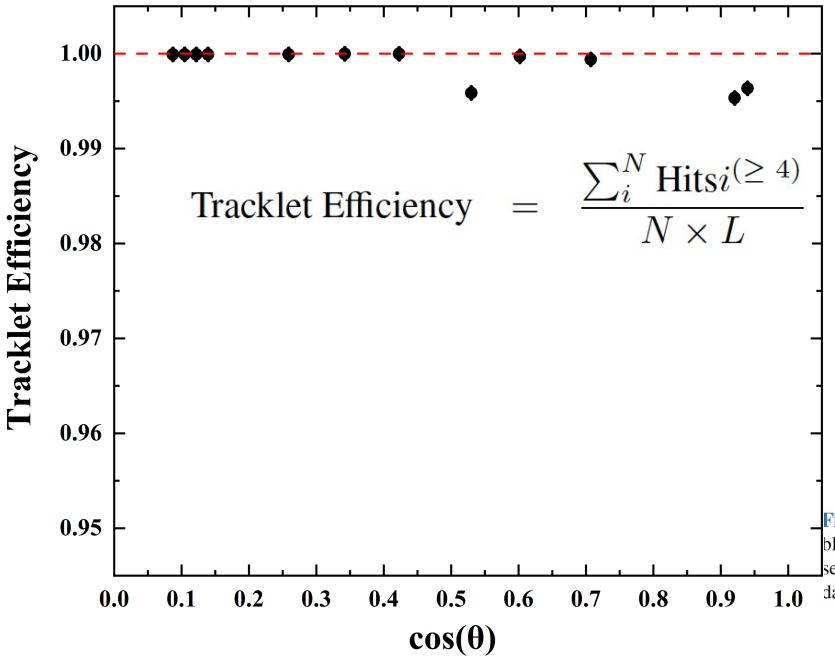


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Number of hits



Tracklet efficiency



RSU design

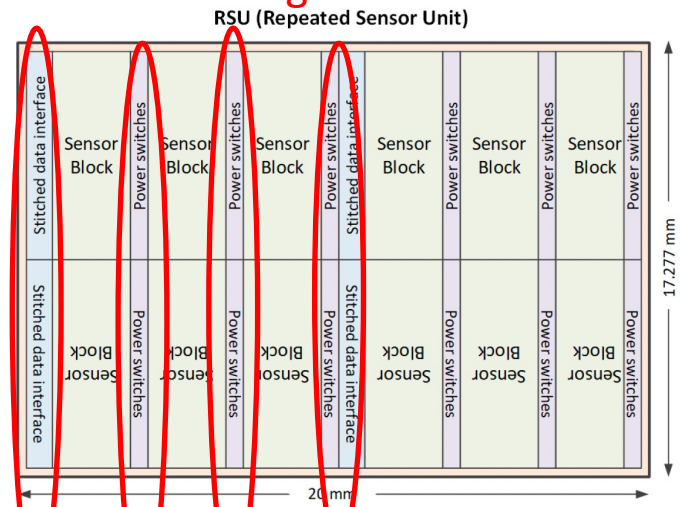


Figure 4.50: Proposed floor-plan for a repeated sensor unit (RSU) (not to scale). It contains several identical senso blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Each sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals and data to the edge of the stitching sensor.

Research team

- IHEP: 8 faculty, 2 postdoc, 5 students
- IFAE: Chip design , Sebastian Grinstein et al
  - CEPC Taichupix chip design, ATLAS HGTD upgrade
- IPHC/CNRS: Christine Hu et al Collaboration in FCPPL and DRD3 framework
  - CEPC Jadepix design, ALICE ITS3 upgrade (especially on MAPS design, stitching)
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: chip design, ladder assembly (2 faculty , 3 students)
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 students)
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing: irradiation study, chip design : (2 faculty, 4 students)

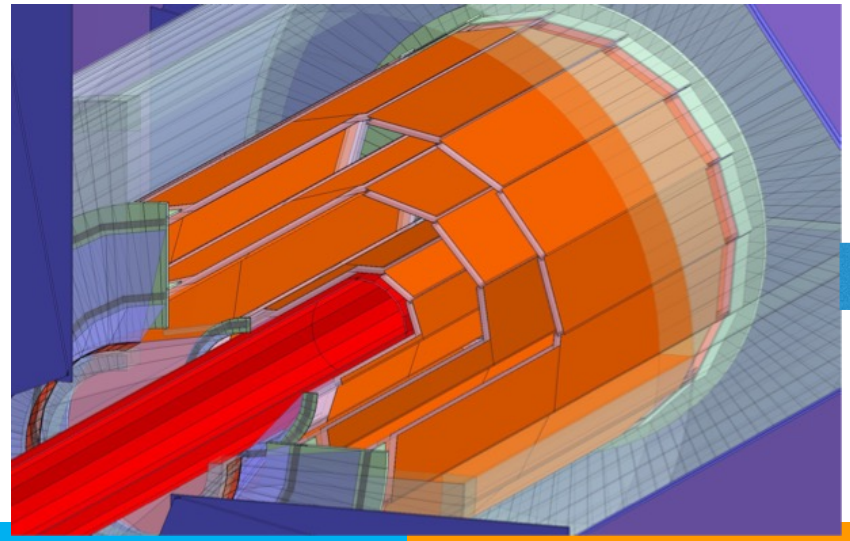
Work plan

- Baseline: work in TJ180 and TPSCO65nm to develop stitched MAPS
  - 1st stitching prototype with TJ180 (2025-2026)
  - 2nd stitching prototype with TPSCO65 (2027-2028)
- Exploring HLMC 55nm as secondary supplier
  - Recent Joint R & D collaboration with CERN for ALICE3 tracker upgrade

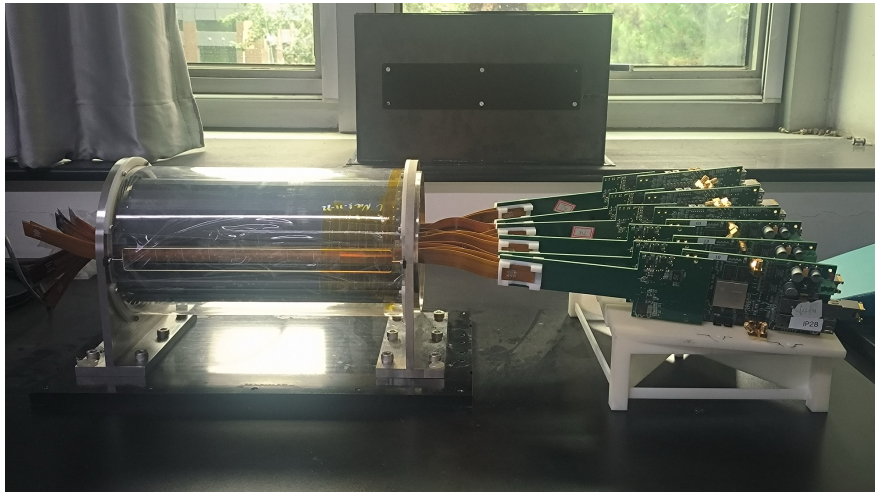
Summary

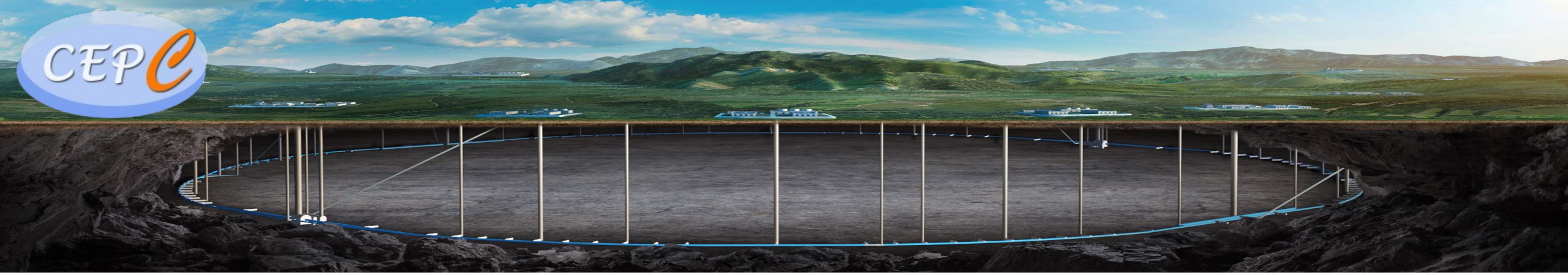
- Working on reference TDR for CECP vertex detector
  - Aiming for stitching technology as baseline design for reference TDR
- We active expanding international collaboration and explore synergies with other projects
  - Recent collaboration with CERN in HLMC55nm technology for ALICE3 tracker upgrade
  - We are member of ECFA DRD3 collaboration

CEPC vertex conceptional design (2016)



CEPC vertex prototype (2023)





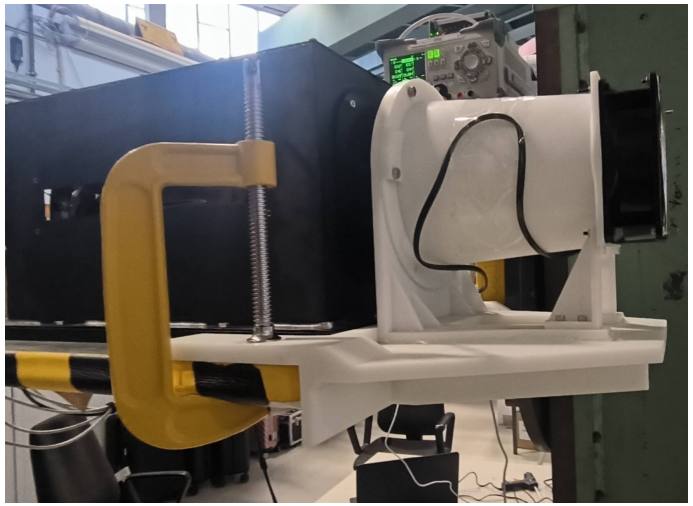
Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

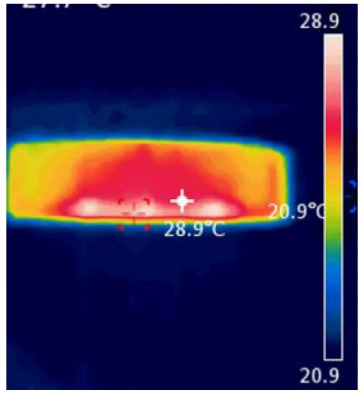
Recommendations
Air cooling experiments in DESY testbeam

- Dedicated air cooling channel designed in prototype, tested in DESY testbeam
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm^2 (17.5 MHz in testbeam)
  - Before (after) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan

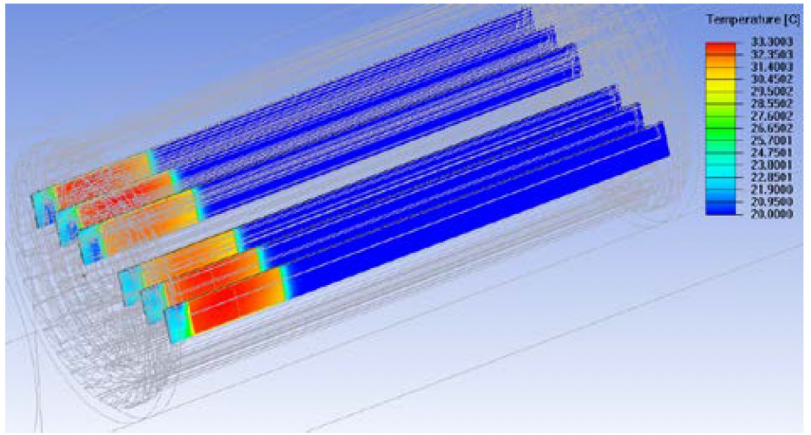
Vertex detector prototype in DESY testbeam



Chip temperature under cooling during beam test: Max 28.9 ℃



Prototype cooling simulation： Max 33.3 ℃



Summary: working plan

- CEPC vertex detector timeline is about 3-4 years after AlICE ITS3 upgrade
  - It will benefit from experience from AlICE ITS3 upgrade

	CEPC Final goal	CEPC Expected date	AlICE ITS3 schedule
CMOS chip technology	65nm CIS	2028 Full-size 65nm chip	2025
Spatial resolution	3-5 μm with final chip	2028	2025
Stitching	65nm CIS stitched sensor	2029	2026 wafer production
Bent silicon with small radius	Bent final wafer with radius ~11mm	2030	2027
Detector cooling	Air cooling with full power	2027： thermal mockup	2027
Detector integration	Detector with bent silicon design	2032	2028