Upgrade of the Belle II Vertex Detector with depleted monolithic CMOS active pixel sensor

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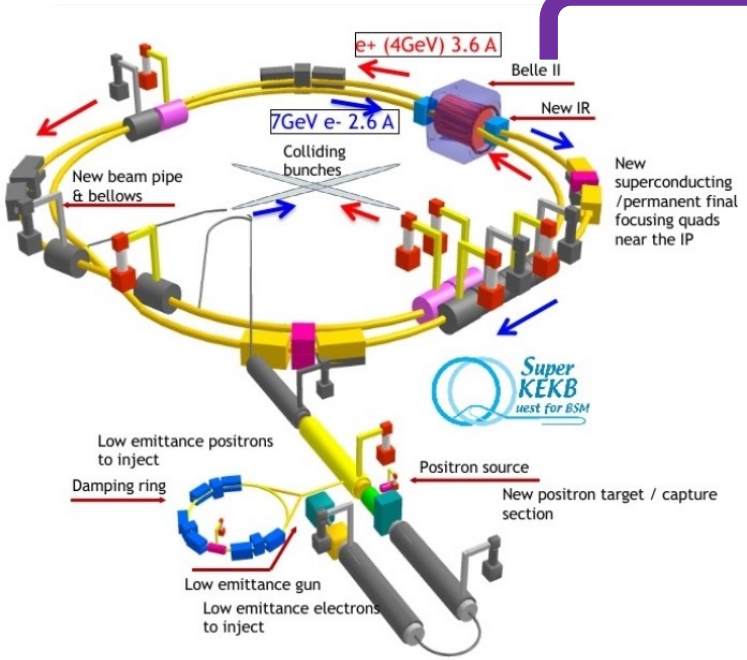
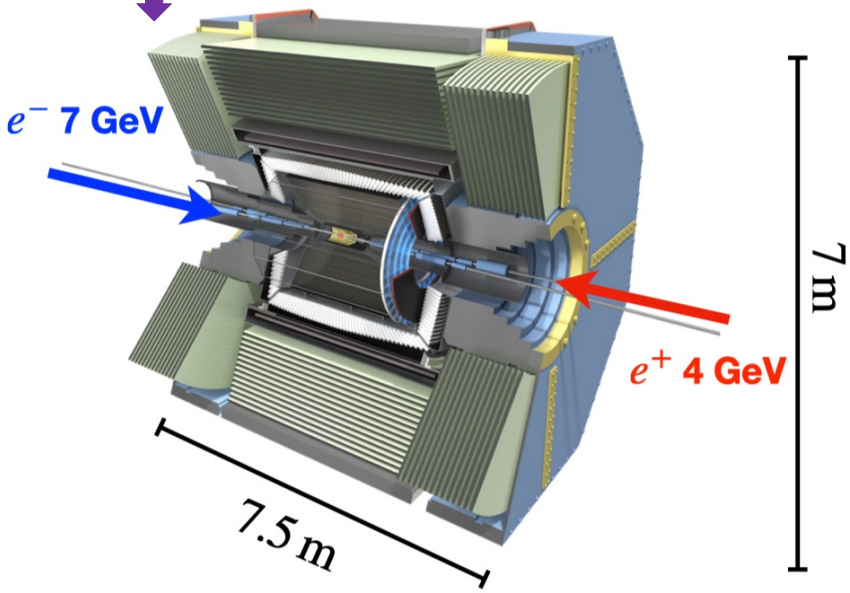
On behalf of the Belle II VTX collaboration

SuperKEKB and Belle II





SuperKEKB collider

- ❑ Asymmetric e^+e^- collisions at Y (4S) resonance at 10.58 GeV
- ❑ Start from 2019, Long shutdown 2022/23, Run2 since 2024
- ❑ Achieved luminosity 575 fb^{-1} with 5.1E34 $cm^{-2}s^{-1}$ (target: 50 ab^{-1} , 6E35 $cm^{-2}s^{-1}$)

Belle II: FWD - BWD asymmetric onion-shaped detector

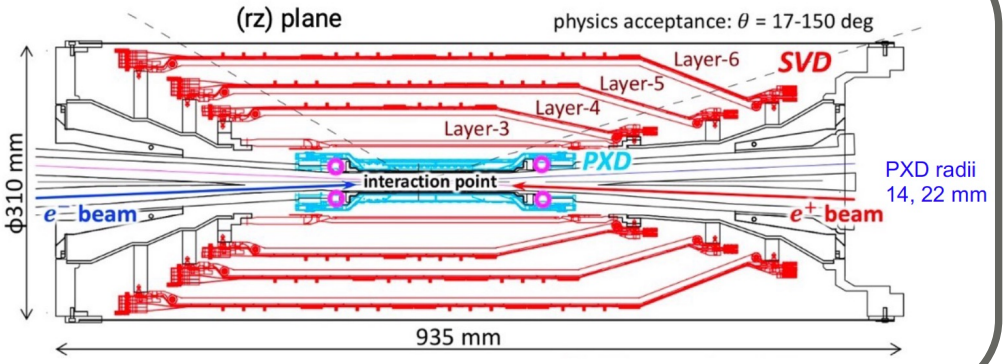
- ❑ KL and Muon Detector
- ❑ EM Calorimeter
- ❑ Particle ID Detector
- ❑ Central Drift chamber
- ❑ Vertex Detector

Current vertex detector (VXD)

Current VXD consists of:

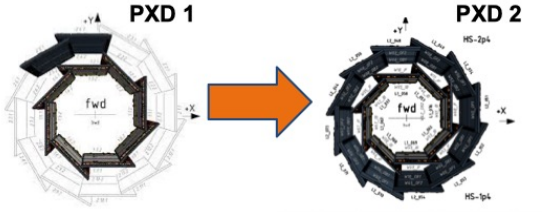
- 2 inner layers of Pixel Detector (PXD) using DEPFET pixel sensors
- 4 layers of Silicon Vertex Detector (SVD) using double-sided strip sensors

Excellent performance with occupancy<1%



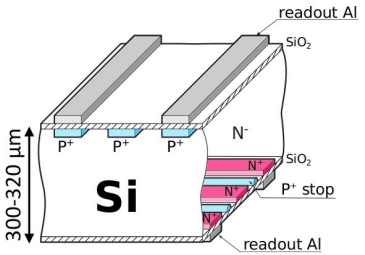
PXD

- Track impact parameter resolution ($\sigma_{r\varphi}$ 10-22 μm, σ_Z 20-40 μm), with 98% efficiency in L1+L2
- Thin sensors (75 μm), 0.21% X_0/layer
- N_2+CO_2 cooling
- Pitch 50-75 μm, Integration time 20 μs
- Occupancy limit 3%



SVD

- Tracking ant PID at low p_T, connection with CDC, hit efficiency > 99%, time resolution 3ns, event T_0
- Thick sensors (300 μm), 0.75% X_0/layer
- CO_2 cooling
- Trigger latency limited to 5 μs by readout
- Occupancy limit 6% (L3)

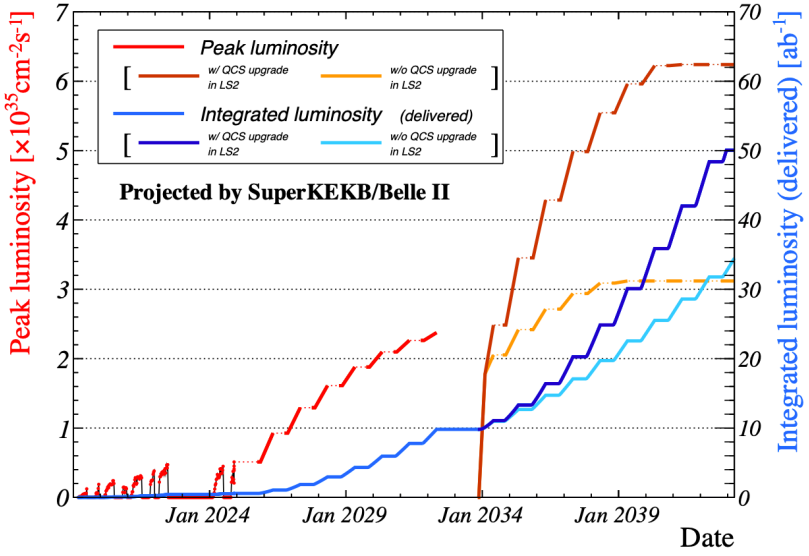


Upgrade motivation

- **Large uncertainty on background extrapolation at target luminosity and with a possible upgrade of the IR:**
  - *MDI design: Final focusing quadrupole QCS inside detector, actually consisting of several magnets (correctors, field cancel magnet,..)*
  - *Possible background mitigation scenarios [ref. CDR]*
- **Damage of switcher increases currents ⇒ Increased current increases temperature**
- **Limited safety margin and performance degradation in high background scenario**
  - *PXD layer 1: up to 2% occupancy (32 MHz/cm^2)*
  - *SVD layer 3 up to 9% occupancy (9 MHz/cm^2)*

At target luminosity we may reach the limits of current detector

⇒ need higher granularity and time resolution in all layers



LS2 around 2032

VTX proposal

Initial Requirements:

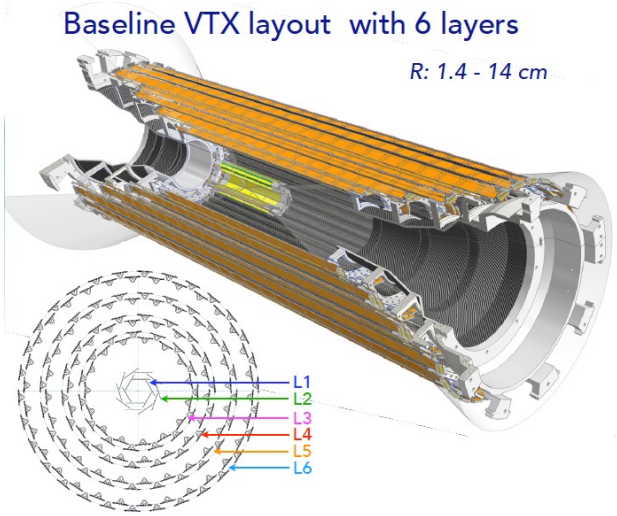
- Spatial resolution < 15 μm results in 30 - 40 μm pixel pitch
- 50 - 100 ns timestamp resolution
- 120 MHz/cm² hit rate
- 300 mW/cm² power dissipation
- Total material budget < 3.5% X_0
- Operation simplicity and reduced services
- Same size / volume as current Belle II VXD, replacing both PXD and SVD
- Radiation tolerance level: TID: ~ 100 Mrad, NIEL: ~ 5 × 10^{14} neq/cm²

Six straight layers with **depleted monolithic CMOS active pixel sensor (DMAPS)**:

inner VTX (iVTX, 1-2) and outer VTX (oVTX, 3-6)

Layer	L1	L2	L3	L4	L5	L6	Unit
Radius	14.1	22.1	62.5-69 (*)	82.5-89 (*)	108-114.5 (*)	133.5-140 (*)	mm
#ladders	6	10	30	36	48	60	
#Sensors	4	4	12	16	20	24	/ladder

(*) staggered ladder design with two different radii per layer



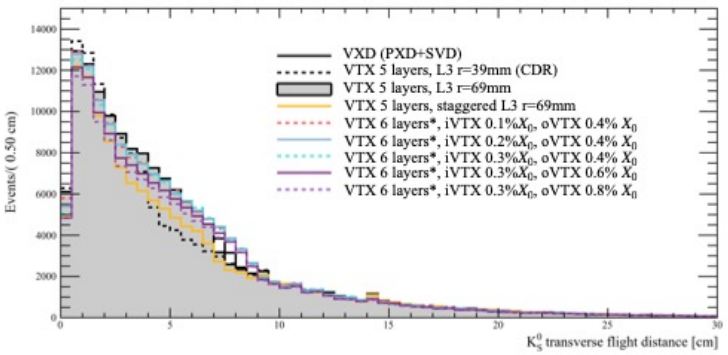
VTX performance optimization

Benchmark physics channels, under different background scenarios are used to assess the VTX performance:

- ❑ 5 vs. 6 layers, with L3 at two different radius
- ❑ Different material budget

The new 6 layers geometry outperforms the previous 5 layers in CDR.

K_S^0 reconstruction efficiency (from $B^0 \to J/\Psi + K_S^0$)



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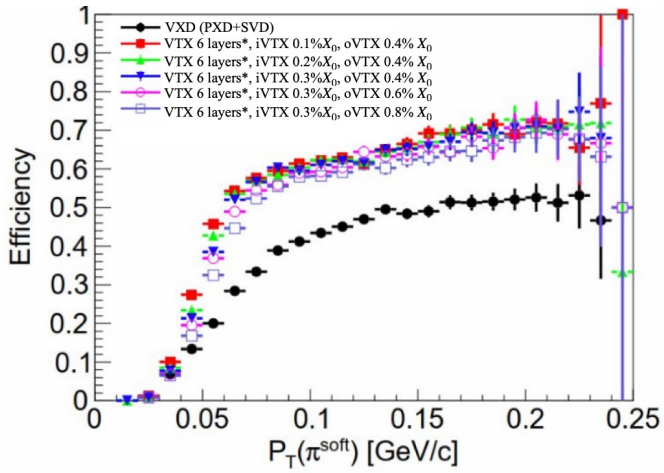
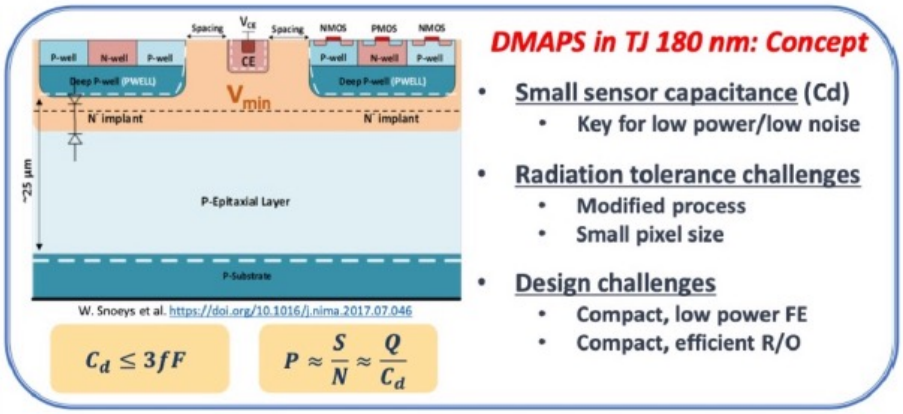
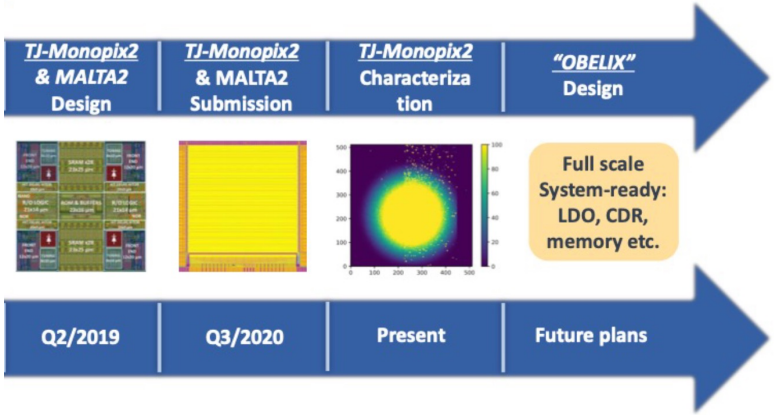


New baseline 6 layers and new material budget (0.3% X0/layer for iVTX and 0.8% X0/layer for oVTX) bring improvements wrt current Belle II VXD

TJ-Monopix2 as starting point

- Designed initially for ATLAS ITK outer layer: now being used as the basis for Belle-II VTX
- DMAPS in modified TowerJazz 180 nm: to improve drift field for improved radiation hardness and faster readout
- Small collection electrode (capacitance < 3fF)
- Chip size: 2× 2 cm²
- 512 × 512 pixels, each 33 × 33 μm² in size
- Timestamping: 7-bit LE/TE (ToT) @ 25 ns
- Column drain readout capable >>120MHz/cm^2 (triggerless)
- Different bulk materials: High-resistivity epi layer: 1-8 kΩ cm @30µm, Czochralski
- Different front-end flavors (AC or DC coupling of detector input in amplifier)

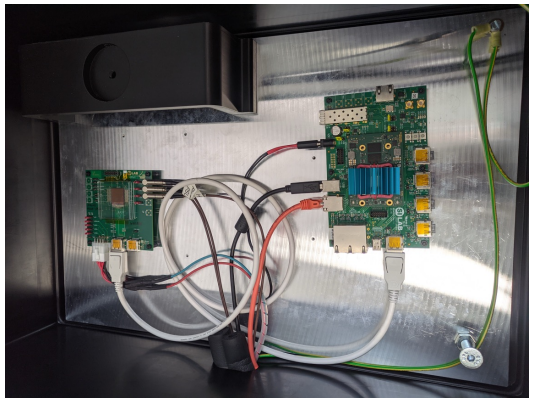


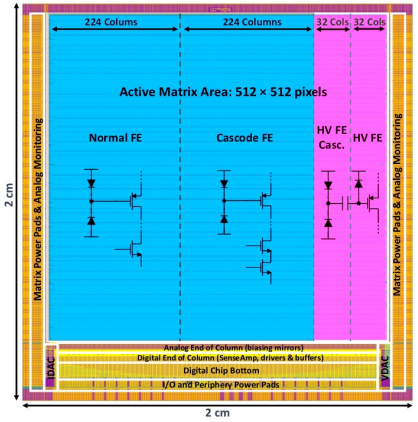


Key element for the choice of TJ-Monopix2 is the demonstrated performance of radiation tolerance

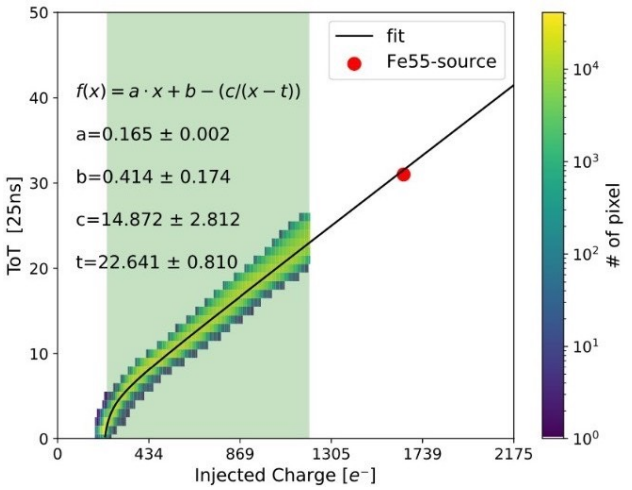
TJ-Monopix2 characterization

- DAQ System: BDAQ53, based on RD53 chip readout: One DAQ board can connect several FE boards
- Exclusive operation: blue or magenta region, not both





- Detailed characterization of TJ-Monopix2 (all FE variants) to validate key performance crucial for OBELIX design
  - ToT calibration,
  - Source tests
- Comparison measurements vs. simulations



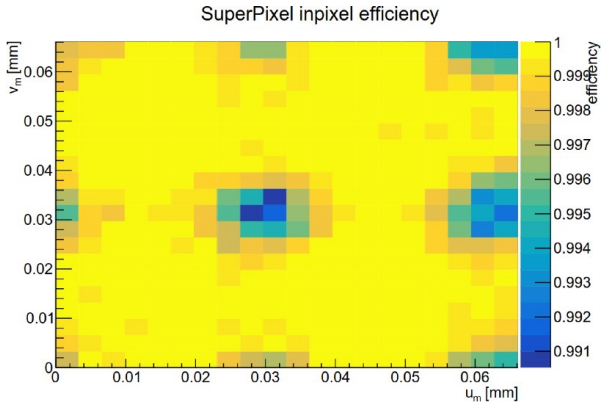
TJ-Monopix2 test beam result

Several beam test campaigns at DESY (3-5 GeV electrons)

- **July 2022:** non-irradiated sensors and high threshold 500 (un-tuned chips)
  - *Efficiency ~99%*
  - *position resolution ~9 μm*
- **July 2023:** low threshold (250-300) and irradiated sensor (5×10^{14} n_{eq}/cm^2 with 24 MeV protons)
- **July 2024:** repeat on p-irradiated sensor with high fluence
  - *TID (100Mrad): both DC and AC cascode efficiency 99.9%*
  - *NIEL 5×10^{14} n_{eq}/cm^2 : slightly worse efficiency than in TB 2023 (effect of higher T and higher leakage current is the explanation)*
- DC cascode efficiency>99.5% but ~3% of masked pixels
- AC cascode efficiency ~98.5%

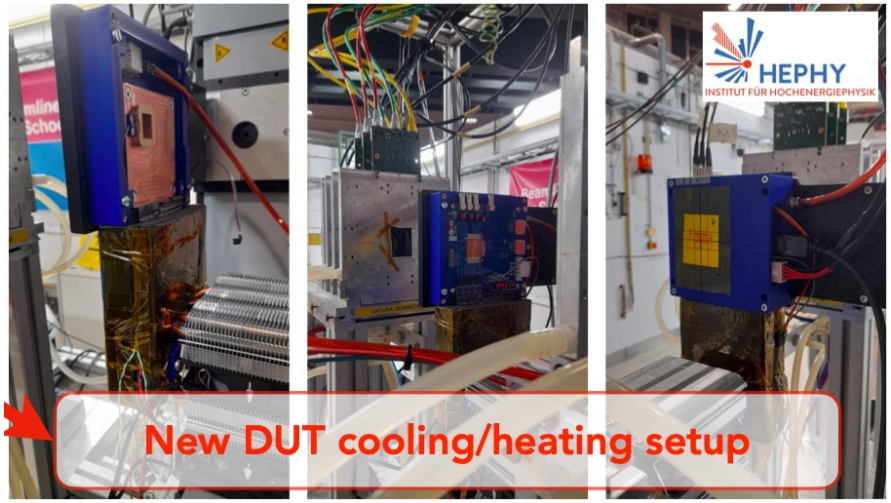
Results TB July 2023

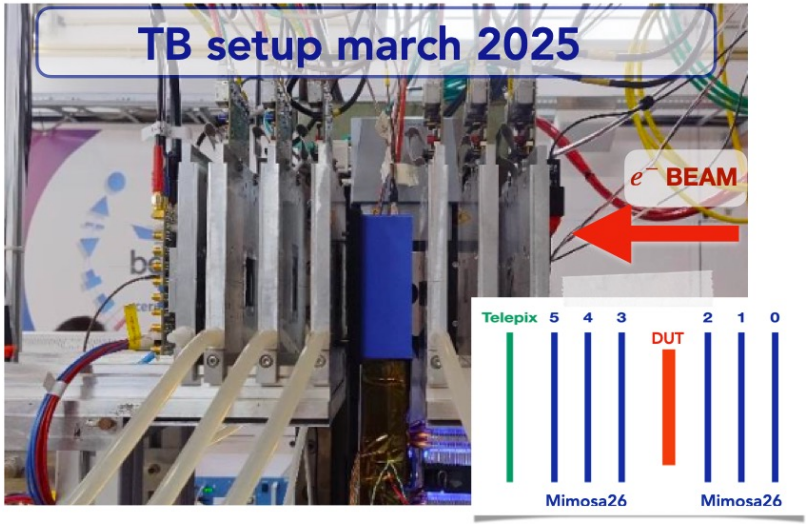
FE amplifier	Coupling	Efficiency [%]
Normal	DC	99.99
Cascode	DC	99.79
Normal	AC	98.11
Cascode	AC	99.13



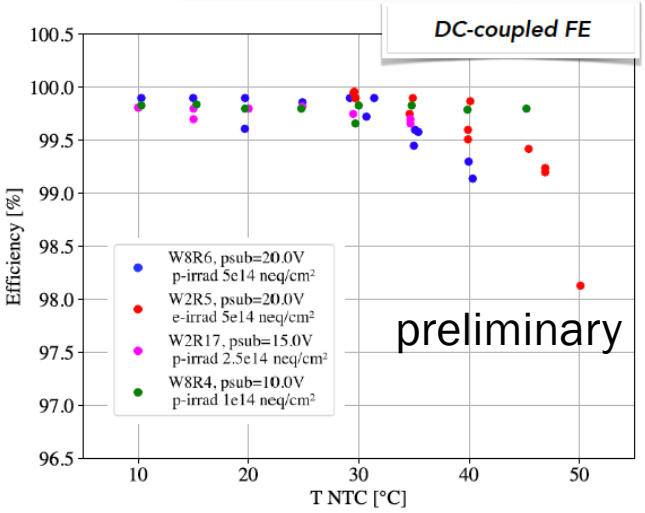
TJ-Monopix2 test beam 2025

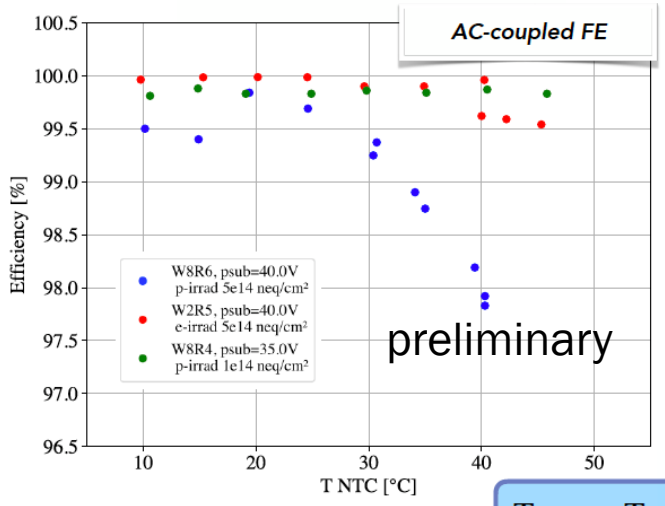
Peltier cell:





Efficiency vs Temperature for same FE settings at max bias



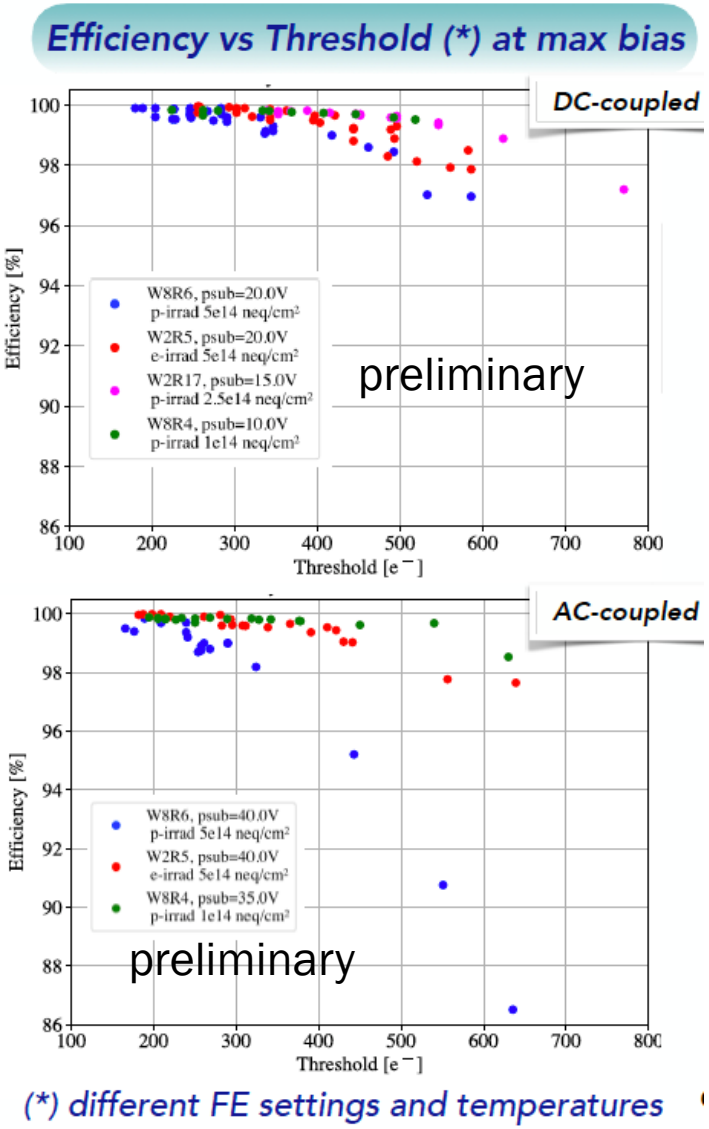


- Efficiency degrades with temperature after irradiation, especially for AC-coupled FE
- DC-coupled remains >99% efficient up to ~40 °C

$T_{Chip} \sim T_{NTC} + 7°C$

TJ-Monopix2 test beam 2025

- Efficiency depends on irradiation level: Less irradiated chips show higher efficiency, even at higher thresholds
- e- irradiated chip has clearly higher efficiency than the p-irradiated chip at the same fluence (NIEL 5*10^4 n_{eq}/cm_2), suggesting lower bulk damage
- At the same threshold p-irradiated chip (NIEL 5*10^4 n_{eq}/cm_2) shows stronger degradation on AC- compared to DC-coupled frontend

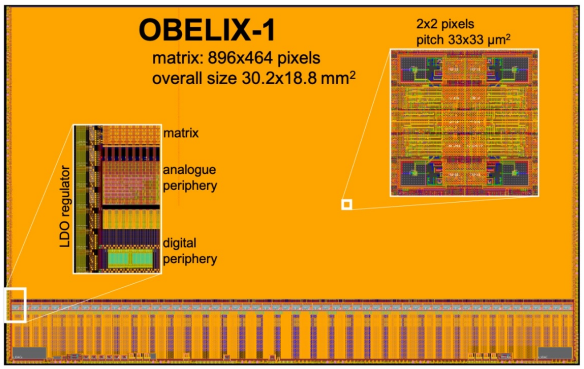


The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Optimized BELle II pIXel sensor design

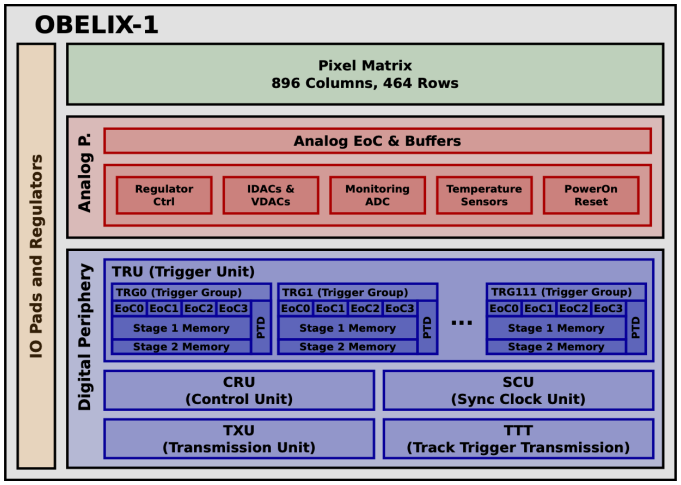
Analog matrix inherit from TJ-Monopix2 with Belle-II-specific adaptions like:

- Geometry
- Trigger logic and buffer memory
- Powering (on-chip LDO voltage regulators)



Specifications:

- Chip size: 30 x 19 mm²
- Pixel: 33 x 33 µm² / 464 rows, 896 columns
- Time stamping: 50 to 100 ns
  - PTD: Fine time stamping ~5ns
- Allows ~10 µs trigger latency at 30kHz
  - TTT: Trigger output ~10 ns resolution
- Hit rates up to 120 MHz/cm²



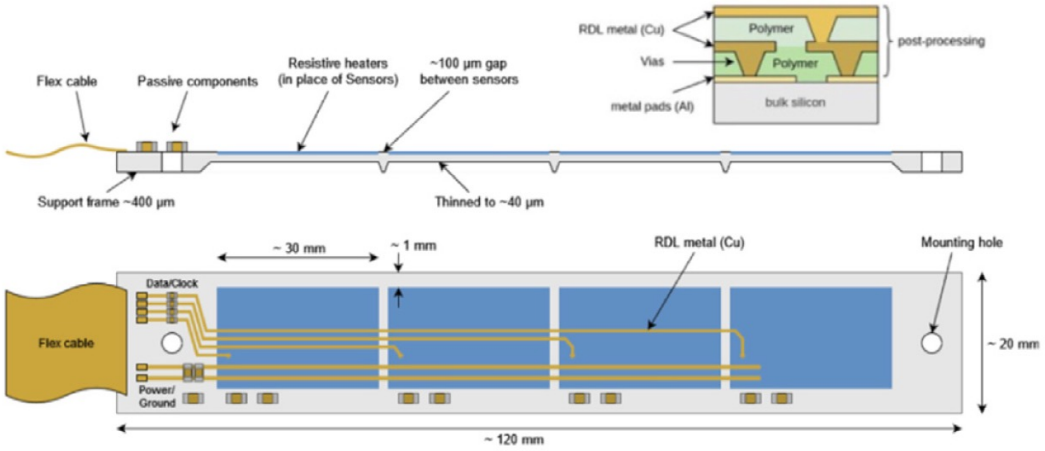
iVTX design

Self-supported all-silicon module

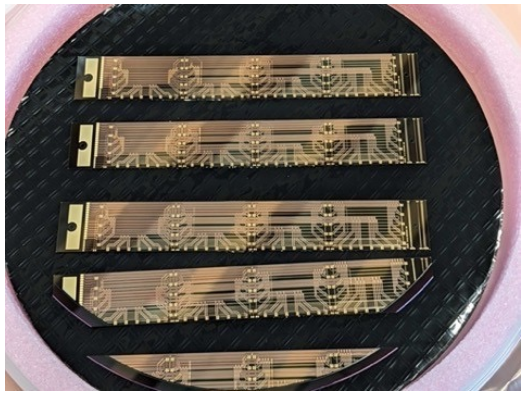
- 4 contiguous sensors diced out of wafer => 12 cm long
  - Insensitive distance from adjacent pixel matrices ~ 500 µm
- Interconnected with redistribution layer
  - 2 metal layers
  - Single connections at ladder end

Material budget:

0.3% X_0 (water and graphite-based)

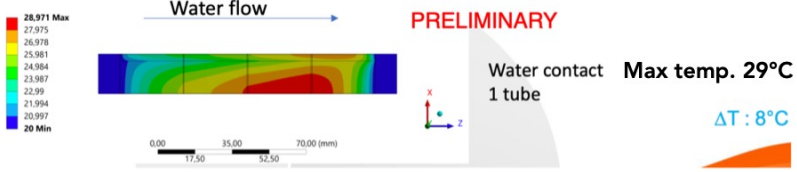


Initial iVTX ladder concept compatible with air cooling

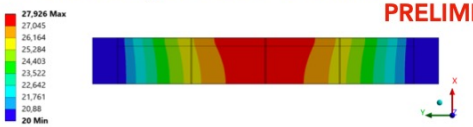


First dummy wafers with redistribution layer

Preliminary results liquid cooling simulation



Preliminary results thermal conduction simulation

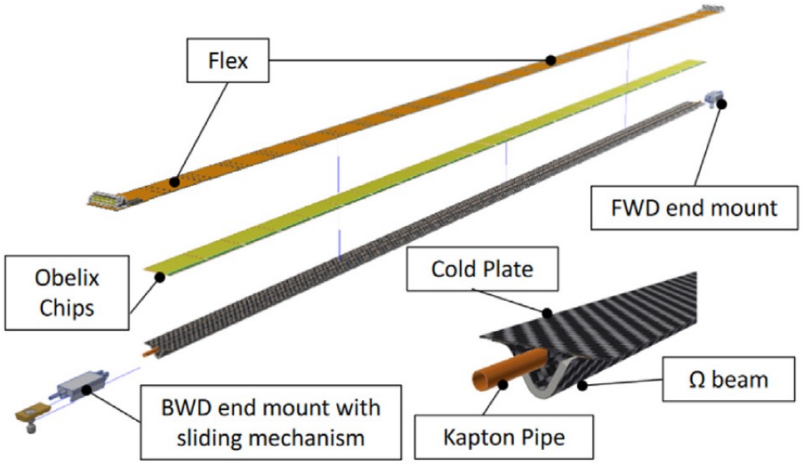


Perfect thermal contact between Si and the TPG layer

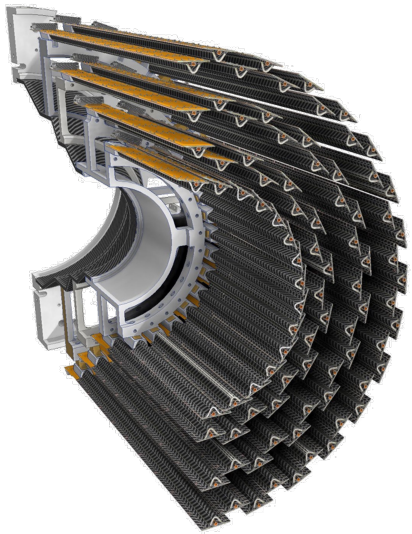
oVTX design

Long and light staves
(similar concept as ALICE-ITS2)

- Used for layer 3 to 6 (82-140mm radius)
- material budget 0.6-0.8% X_0
- Carbon fiber support frame
  - Rohacell core
  - Possibly truss structure
- Cold plate with coolant tube
  - With 200-300 mW/cm^2 => T_{max} < 30˚C, ΔT(1 sensor) ~4 ˚C
- Long flex for power & data
  - 12 sensors read out per side

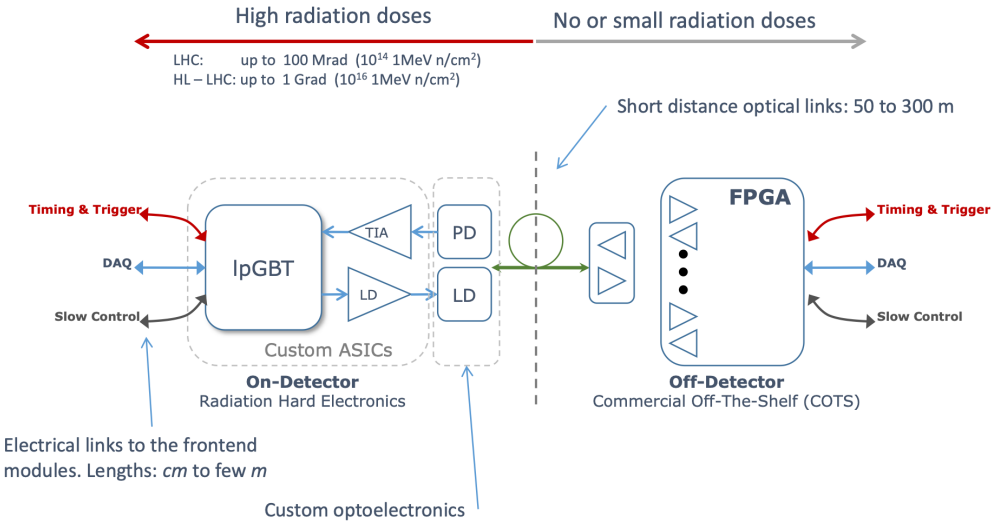


Depending Schematic of the oVTX ladder components with an omega-shaped carbon support.



OBELIX DAQ chain

- CERN lpGPT is considered as transceiver for transmission of DAQ, Trigger and slow control (including VTRX+ optical transceiver)
  - Data with 5.12 or 10.24 Gbps (for uplinks), 2.56 Gbps (for downlinks)
  - I2C, GPIO, 10bit ADC, different DACs
  - Designed for 200Mrad TID
- Will be used at different clock at Belle-II rather intended (LHC)
  - We want to operate at SuperKEKB RF clock / 12 = 508.887 MHz / 12 = 42.40725 MHz
  - Outside specs from developers (39 -- 41 MHz)



Summary

- **Belle II VTX upgrade driven by high occupancy at design luminosity, high beam background and sudden beam loss damage of current DEPFET PXD and DSSD SVD System**
  - iVTX: self-supported all-silicon ladder with RDL
  - oVTX: cooling pipe, flex and CF
- **The OBELIX chip is based on TJ-Monopix2 in 180 nm TowerJazz modified process**
- **Additional features in OBELIX (all on-chip):**
  - Trigger logic (10μs latency)
  - Precision timing module
  - Fast transmission for trigger contribution
  - Voltage regulators, ADC and temperature sensors
- **Development and verification is entering the final stage (submission in winter 2025)**

Thanks very much!

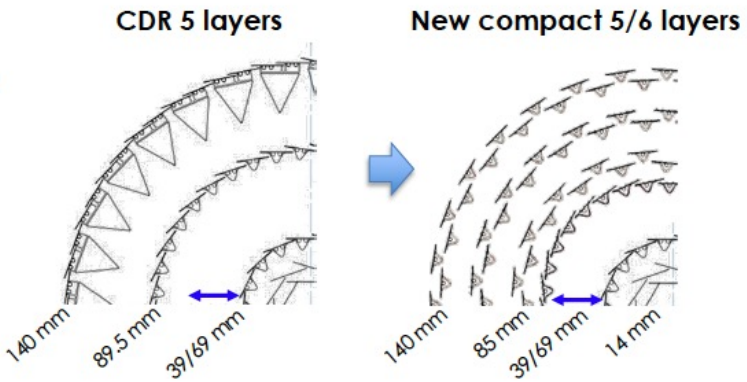
BACK UP

Geometry optimisation

IPHC, Göttingen, Jilin, Pisa, Valencia

Belle II

- CDR recap
  - Initial 5 layer geometry slightly underperforming / K_S^0 reco → understood from too low radius for 1st of 3 last layers
- New geometries (for TDR)
  - Modified oVTX: more compact design and possibly 6 layers
  - More realism
    - Realistic gaps between sensors, implemented with physical size
    - Investigation of material budget range
      L1, L2: 0.1 → 0.2 → 0.3 % X_0
    - Staggered ladders matching compact ladder design
      6 Radii: 14, 22, 39/69, 82.5-89, 106.0-112.5, 133.5-140 mm



- Studies on going in full simulation
  - K_S^0 reco
  - Analysis benchmarking
  } done
  - iVTX X_0
  - L3 distance
  } on-going ot to be done

VTX collaboration

IGFAE, Santiago	Jilin University	IJCLab, Orsay	IPHC, Strasbourg
University of Bergamo	KIT, Karlsruhe	RAL, Oxford	University of Tokyo
University of Bonn	IPMU, Kashiwa	INFN & University of Pavia	KEK, Tsukuba
University of Dortmund	Queen Mary University of London	INFN & University of Pisa	IFIC (CSIC-UV), Valencia
University of Göttingen	CPPM, Marseille	IFCA (CSIC-UC), Santander	HEPHY, Vienna