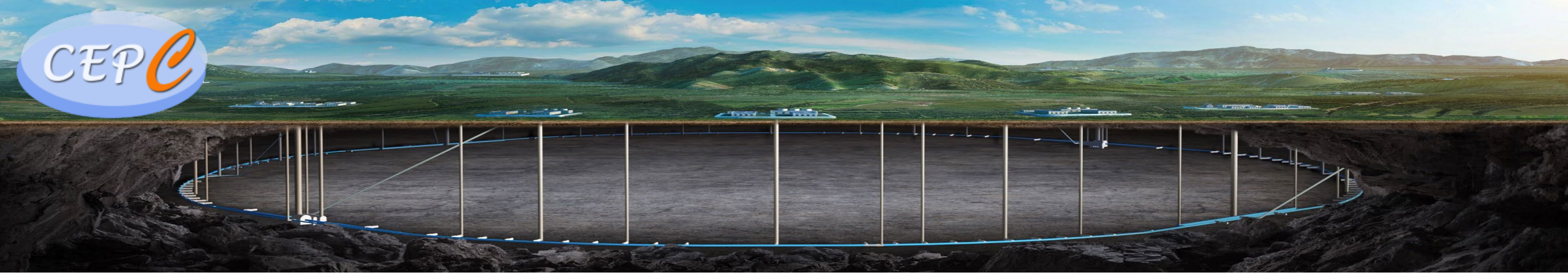


Readout Electronics for the CEPC Reference Detector

Wei Wei
On behalf of the CEPC Elec-TDAQ study team

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

- Introduction
- Requirements
- Technology options and our choices
- Technical challenges
- R&D efforts and results
- Global framework of the electronics system
- Detailed design for common electronics & new FEE ASIC
- Research team and working plan
- Summary

Critical Input from Sub-Det & MDI

	Vertex	ITKB	ITKE	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Chn/chip	512*1024/Stch	512*128		128		128	4~16 @common SiPM ASIC				
Data Width	32bit/hit	42bit/hit		40~48bit/hit		48bit/hit	48bit/hit				
Module Size/Link	168.15cm^2 Half Inner layer	56.00cm^2 14 chip/module		128.00cm^2 8*4cmSensor/module		461.44cm^2 Module size	856 chn Dual-end bar @1.5cm with 0.1MIP th		600 GS 120 cell*5 PCB/Aggr Brd		Aggr Brd
Higgs Bkg (MHz/cm^2)	3.75	9.45e-4	3.60e-3	5.55e-4	1.41e-3	4.80e-3	2.70e-2	0.12	3.00e-4	1.05e-2	5.25e-6
Higgs Data rate/Link(Mbps)	2.02e4	2.22	8.45	3.41	8.63	1.06e2	1.11e3	4.93e3	8.64	3.02e2	<10
LowZ Bkg (MHz/cm^2)	15.00	1.50e-3	6.00e-3	9.90e-4	2.25e-3	4.35e-3	1.95e-2	9.60e-2	9.00e-4	7.50e-3	1.8e-6
LowZ Data rate/Link(Mbps)	8.10e4	3.53	14.11	6.07	13.83	96.4	8.01e2	3.94e3	25.92	2.16e2	<10
HighZ Bkg (MHz/cm^2)	43.50	4.65e-3	0.018	3.00e-3	6.90e-3	1.37e-2	0.06	0.30	2.85e-3	2.40e-2	5.4e-6
HighZ Data rate/Link(Mbps)	2.34e5	10.93	43.24	18.42	42.36	3.03e2	2.47e3	1.23e4	82.08	6.91e2	<10
Detector Channel/module	1882 equiv chips @Stch & Ladder	2376 modules	1236 modules	7040 modules	6368 modules	496 modules	0.96M chn 480 modules	0.52M chn 260 modules	3.38M chn 5536 Aggr Brds	2.24M chn 3072 Aggr Brds	43.2k ch 72 Aggr Brds
Full Data rate @Higgs (Gbps)	2.22e3	5.28	11.08	24.01	54.97	52.73	5.18e2	9.22e2	47.83	9.28e2	<1
Full Data rate @LowZ (Gbps)	8.90e3	8.38	17.45	42.71	88.03	47.77	3.74e2	7.37e2	1.43e2	6.65e2	<1
Full Data rate @HighZ (Gbps)	2.57e4	25.96	53.45	129	270	150	1.15e3	2.30e3	4.54e2	2.12e3	<1

- 1.5 safety factor used for bkgrd rate; VTX includes synchrotron radiation, others not considered

Consideration on global framework of Elec-TDAQ

- Two main stream frameworks for the electronics-TDAQ can be simply categorized as full data transmission (FEE-Triggerless readout) & readout with conventional trigger
- Comparison on main aspects

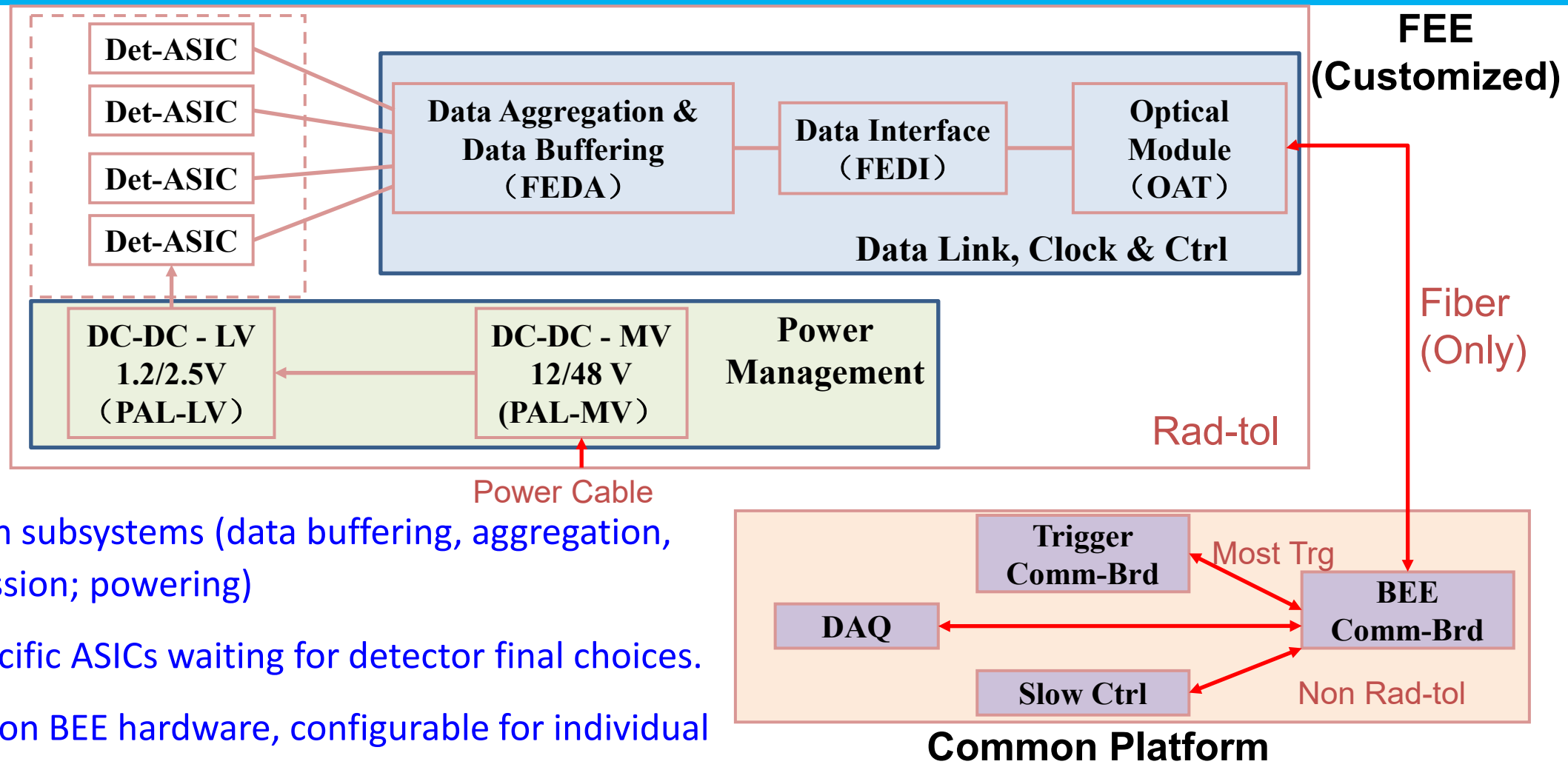
	Full data transmission	Conventional Trigger	Superiority
Where to acquire trigger info	On BEE	On FEE	Full data transmission
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	Conventional Trigger
Maturity	Mature but relatively new	Very mature	
Resources needed for calculation	High	Low	
Representative experiments	CMS, LHCb, …	ATLAS, BELLE2, BESIII, …	

Our choice on global framework

- We choose **Full Data Transmission (Frontend Triggerless) + Backend Trigger** as our baseline global framework, while keep conventional trigger (to be explained) readout as the backup :

1. Maintain the maximum possibility for new physics and future upgrades.
   - Readout all the information w/o pre-assumed trigger conditions.
2. Speed-up the FEE-ASIC iteration & finalization process
   - W/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
3. Enable a common platform design for all Sub-Detectors
   - Common BEE Brd, common Trg Brd, common data interface…
   - Scalable based on the detector volume
4. Sufficient headroom for FEE data transmission based on the current MDI background rate
   - 11Gbps per link on FEE (max by ×4 links)

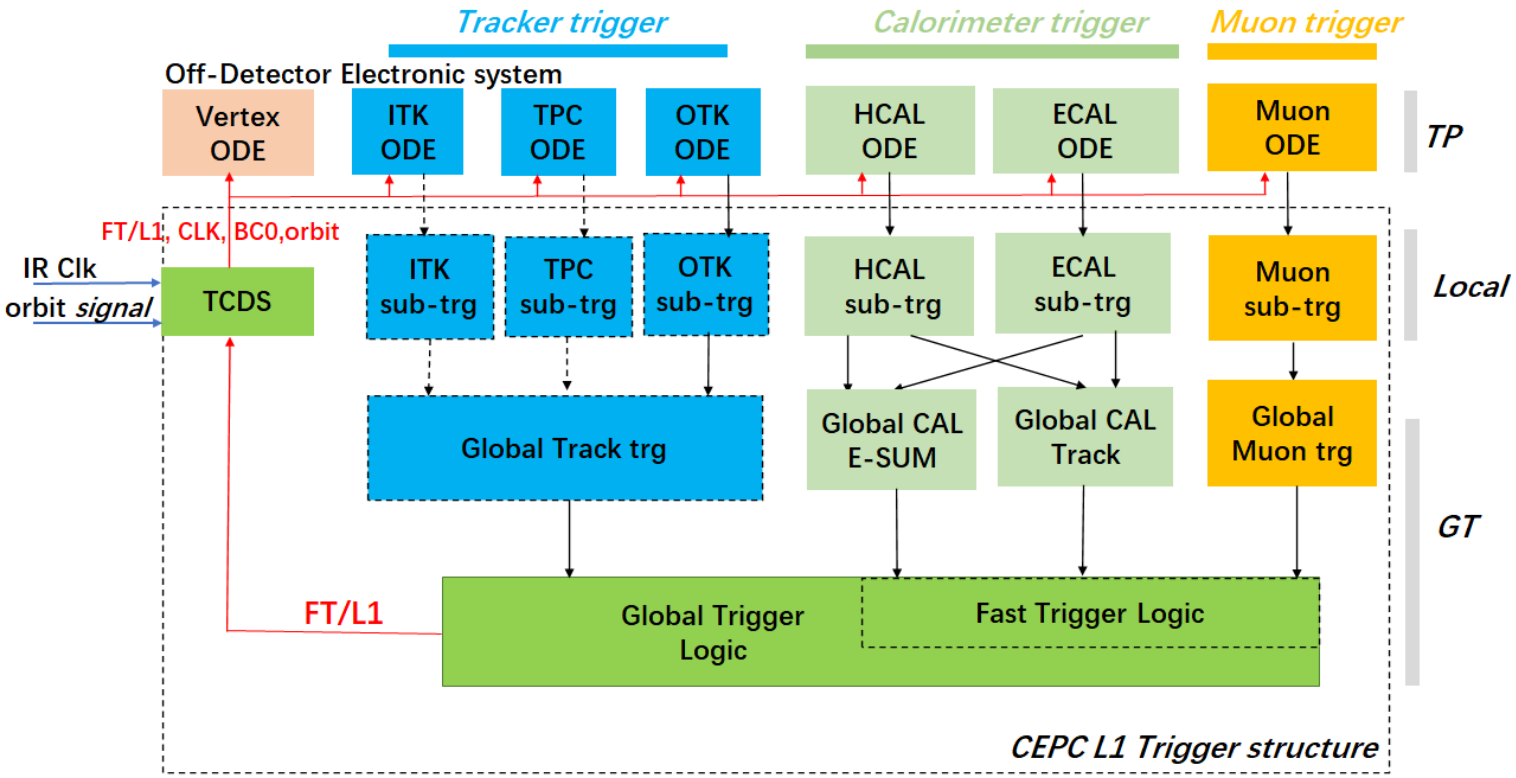
Global framework of the CEPC Elec system



- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choices.
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- Background rate indicated the data link capability can manage the Phase I operation of Higgs & Low Lumi Z in the first ten years
  - Shielding optimization ongoing to suppress the background
  - High Lumi Z situation is still not fully understood, but in the 2nd ten years
    - Replaceable detectors e.g. VTX, ITK.. can be upgraded with new chips with intel-compression and advanced trigger in case
    - Unreplaceable detectors e.g. ECAL, HCAL can be upgraded with more fiber channels

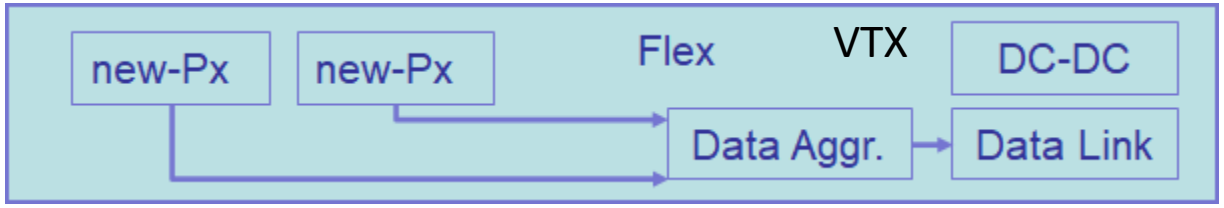


The conventional trigger scheme can serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

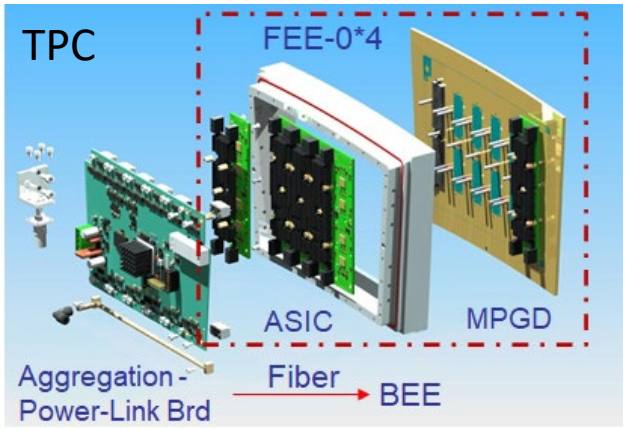
Key Electronics Components

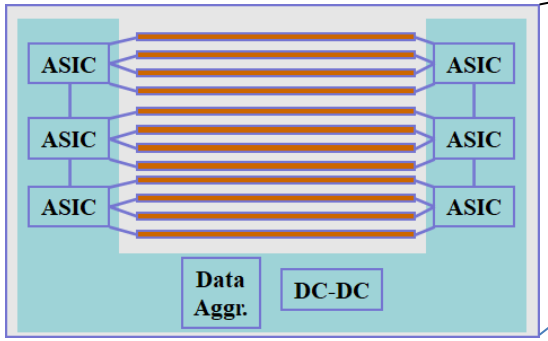
- FEE ASICs for sub-detectors
- Common Data Link
- Common Powering
- Common Backend Electronics
- Alternative Scheme based on Wireless Communication

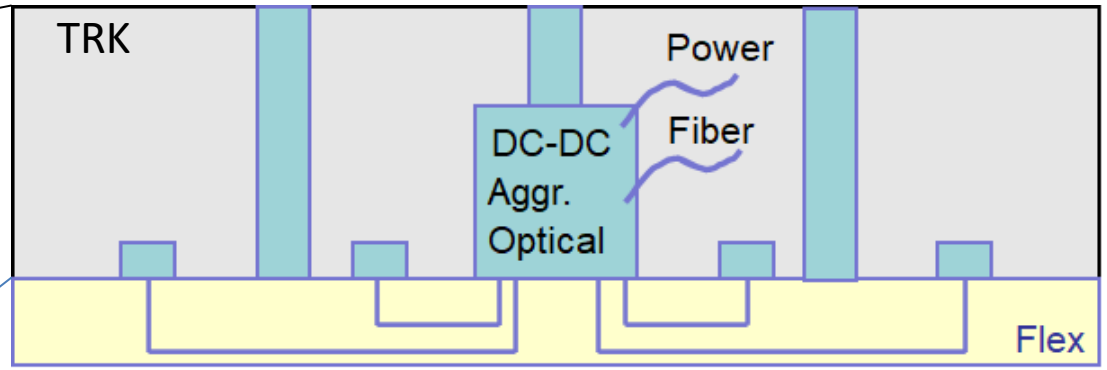
An overview of the Sub-Det readout Elec.

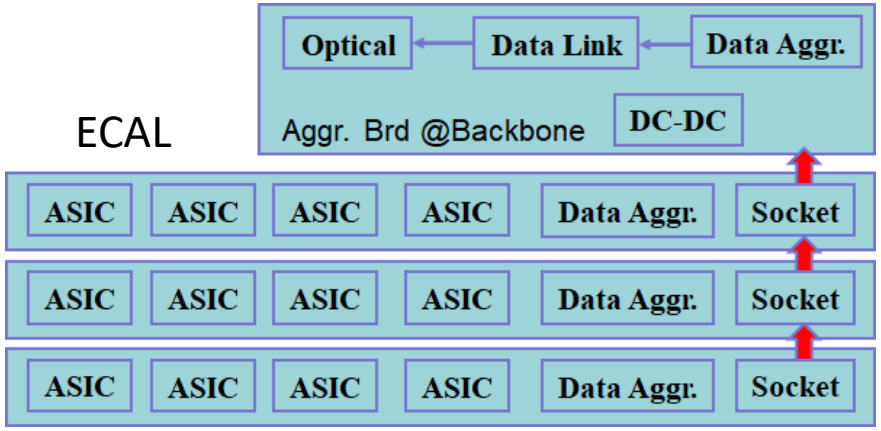


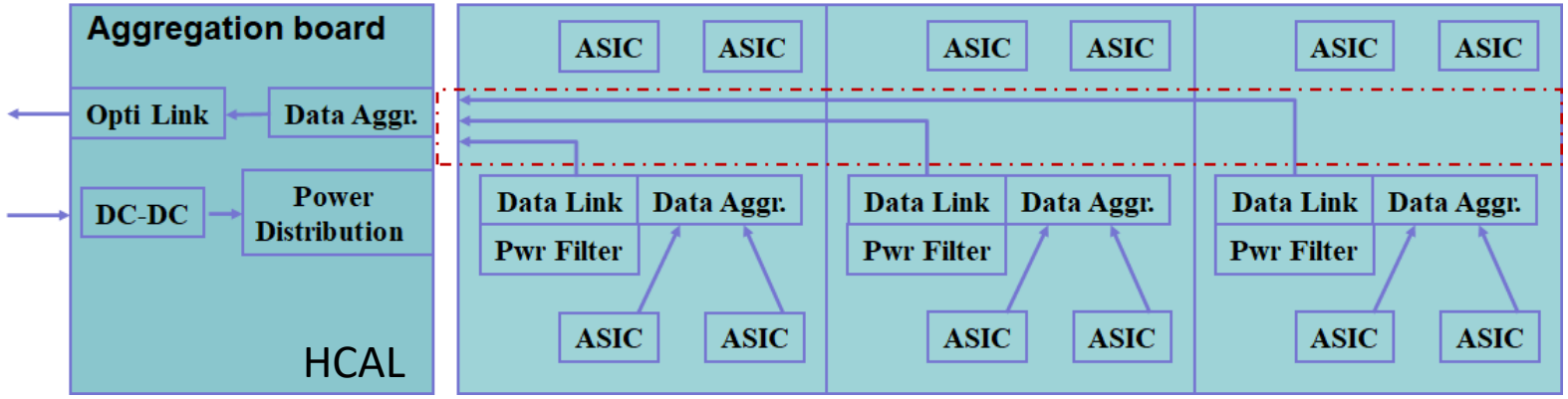
- All sub-det readout electronics were proposed based on this unified framework, maximizing the possibility of common design usage.



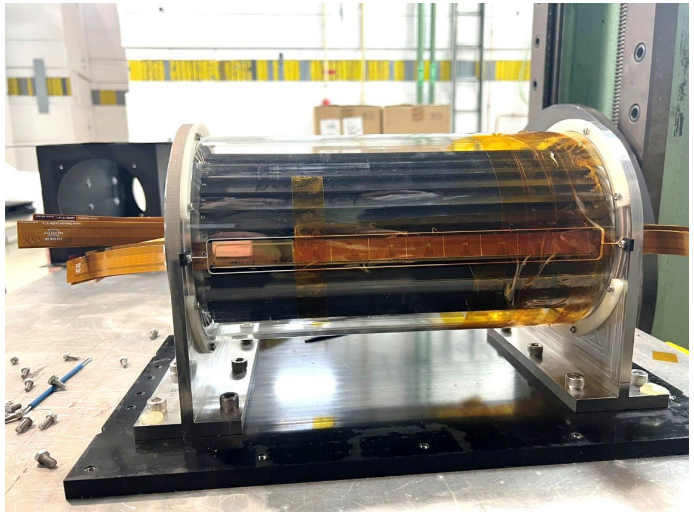




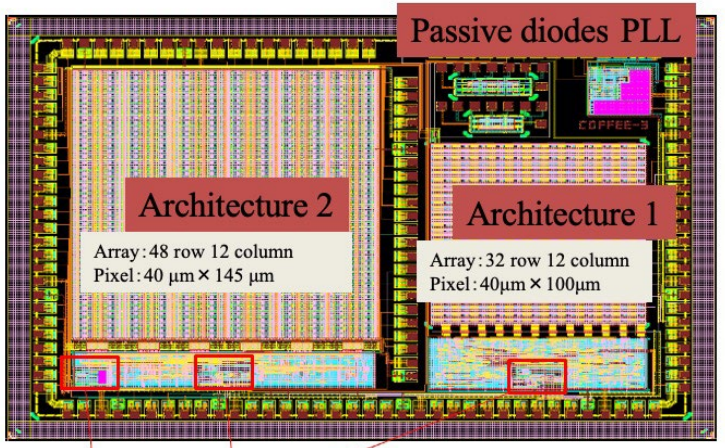




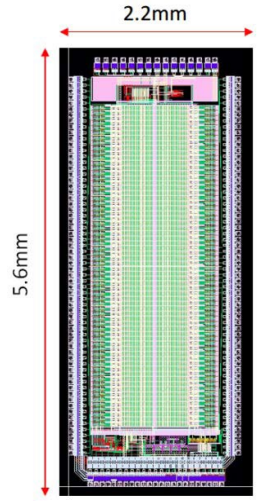
ASICs with R&D and Prototypes

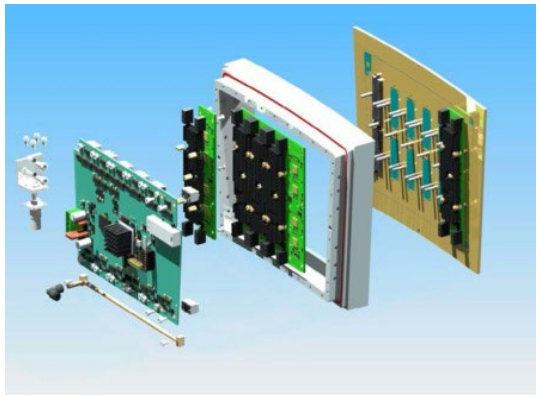


Taichu CMOS Sensor & prototype for VTX

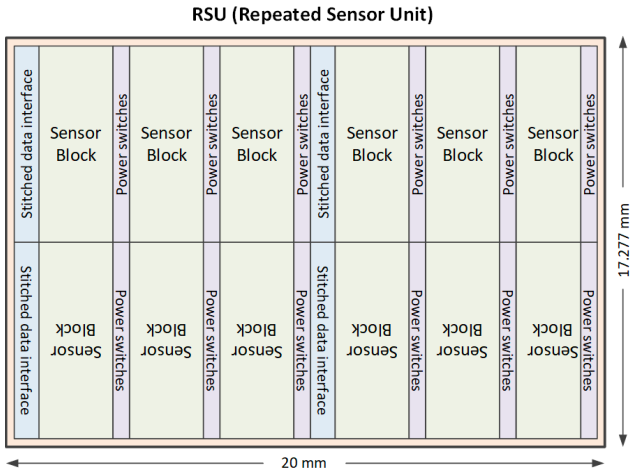


COFFEE HVCMOS Pixel Sensor for ITK

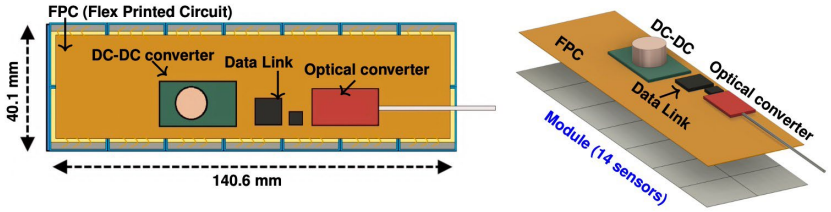




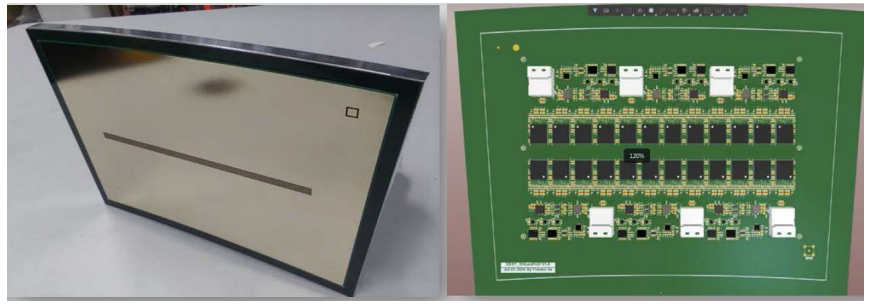
TEPIX ASIC & hybrid module developed for PixTPC



Stitching VTX proposed for CEPC based on Taichu experience

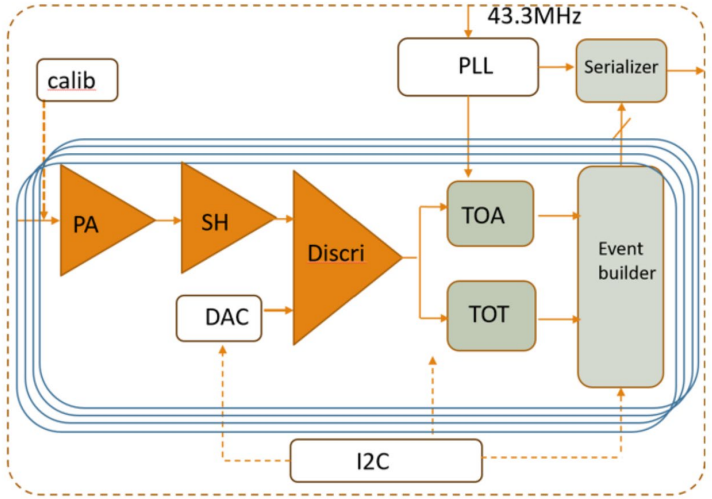


ITK Module based on HVCMOS Pixel Detector

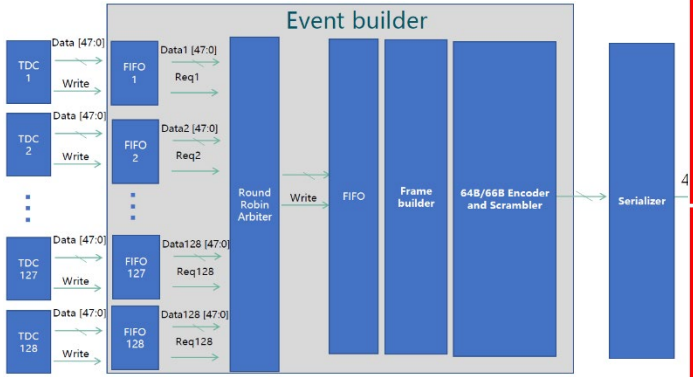


TPC prototype module for beamtest based on TEPIX chip

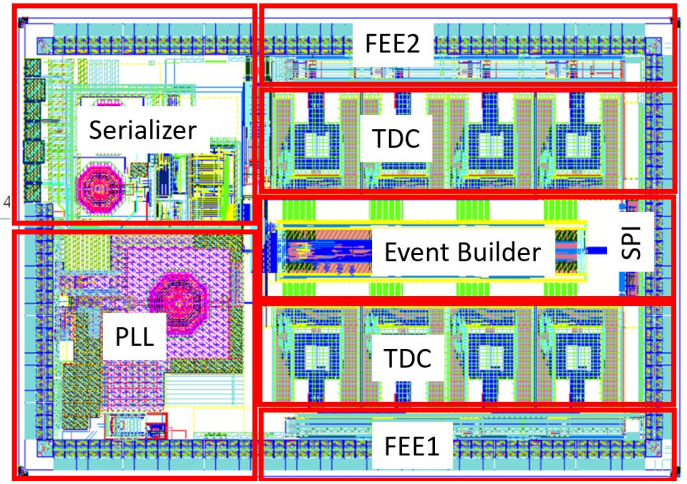
1st ver. in tapeout for the new ASICs



LATRIC ASIC for OTK aiming at high timing precision ~30ps

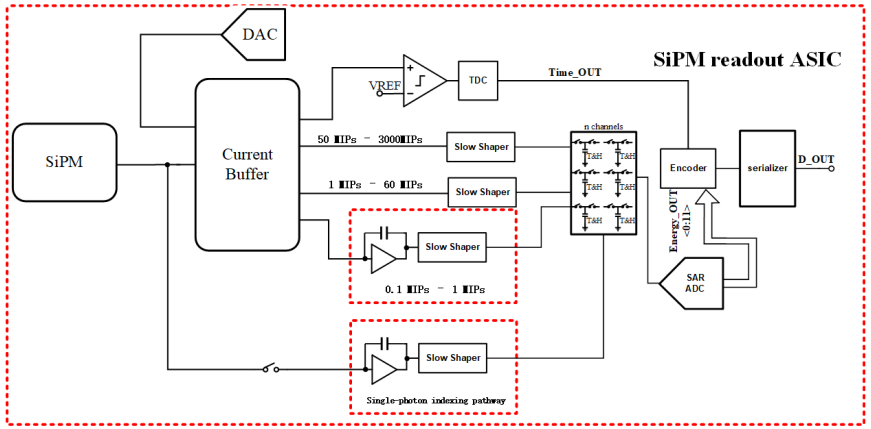


Multi-channel data processing scheme

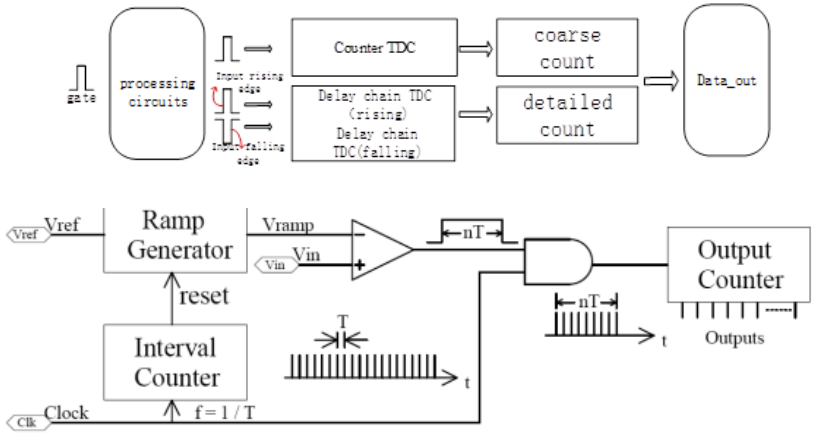


Previous ASIC design for TOF-PET of timing precision ~10ps

- **Design team**
  - **IHEP: 3+2**
  - **CCNU: 2+3**
  - **WTU: 1+1**
  - **HPU: 1**



SIPAC ASIC for the common SiPM readout for ECAL, HCAL & Muon

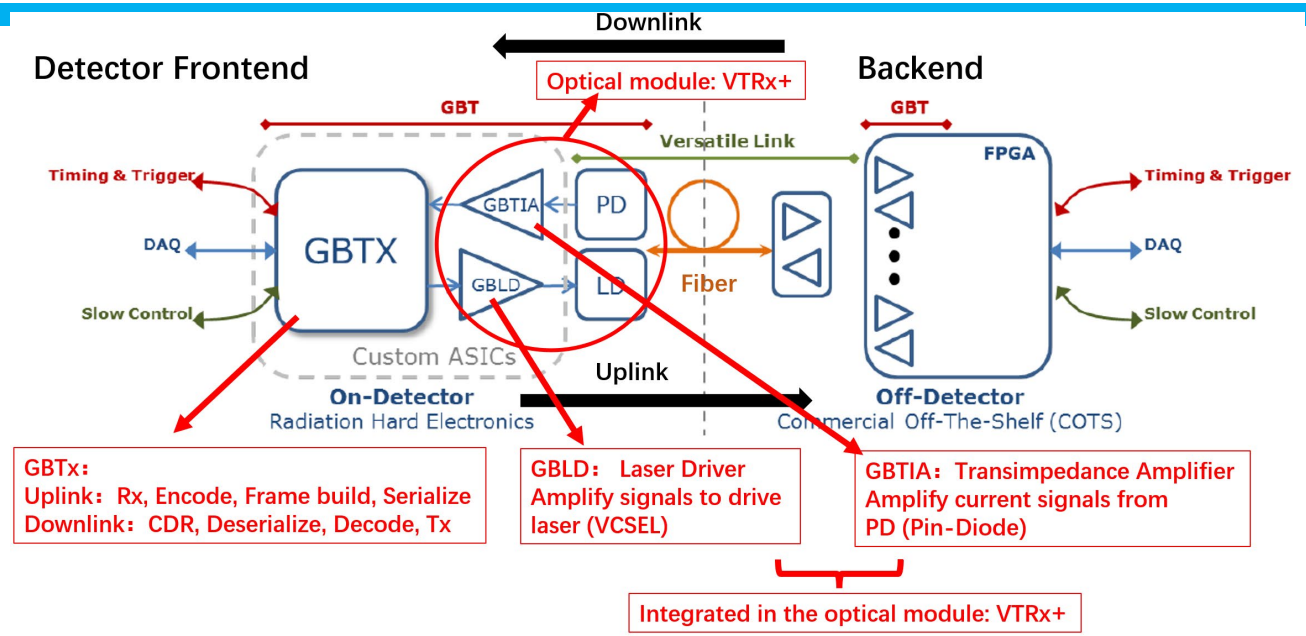


Key blocks including preamp, TDC, ADC all with silicon proven designs

- **Design team**
  - **IHEP: 3+3**
  - **CCNU: 1+3**
  - **NPU: 1+1**
- **Both ASICs have been tapeout in April 7th for the 1st version**

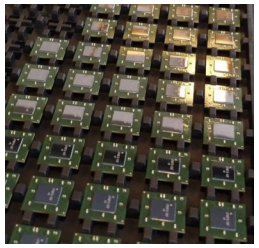
Technical Survey on Data Transmission System

- GBT Project:
  - The lpGBT & VTRx chip series, developed by CERN, are widely used by LHC experiments, as a common project
  - Core components:
    - GBTx: Bidirectional Serdes ASIC
    - GBLD: Laser driver
    - GBTIA: Transimpedance amplifier
    - Customized Optical Module
  - However the base clock frequency of CEPC 43.3MHz is not compatible with lpGBT system
- Our choice:
  - Build a GBT-like universal bidirectional data transmission system
  - Take the lpGBT as a reference, the protocol can be a minimum & necessary set for the readout, clocking & control

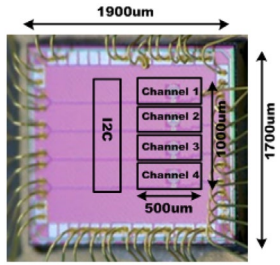


GBT Architecture Developed by CERN

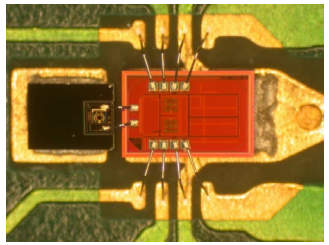
Ref. P. Moreira, The GBT Project, 2007



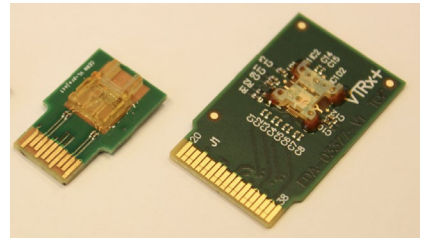
lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps



GBLD (LDQ10)
10.24 Gbps x 4ch



GBTIA
2.56 Gbps

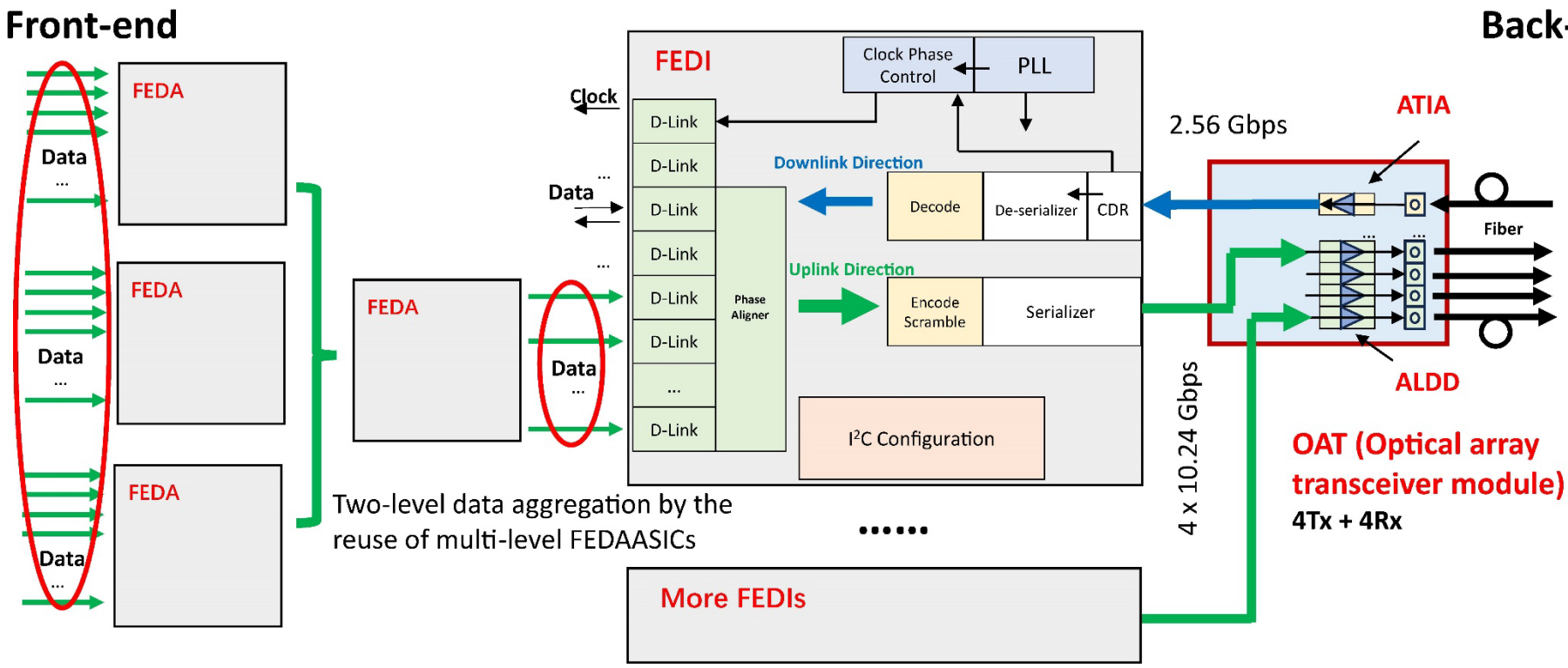


VTRx+
4Tx + 1Rx
Array Optical Module

GBT Series ASICs and optical module

Ref. P. Moreira, GBT Chipset Status and Production Plans, 2013

Detailed design on Data Transmission Structure

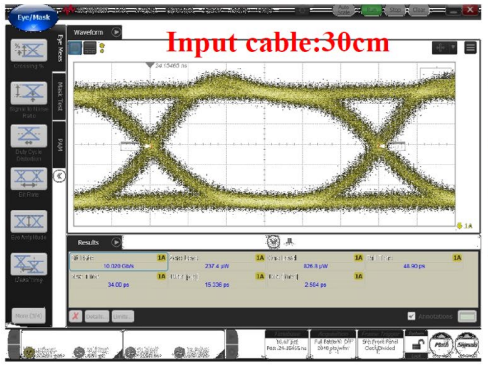


- **Design Team**
  - **IHEP:3 + 3**
  - **CCNU:2+8**
  - **NPU:2+2**
  - **USTC:1+2**
  - **WTU:2+2**
  - **IPAS:1+1**
  - **HPU:1+2**

- Pre-Aggregation ASIC (FEDA): Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like Data Link ASIC (FEDI): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …
- Array Laser Driver ASIC (ALDD) + TIA ASIC (ATIA) + Customized Optical module (OAT)

R&D efforts and results on Data Link

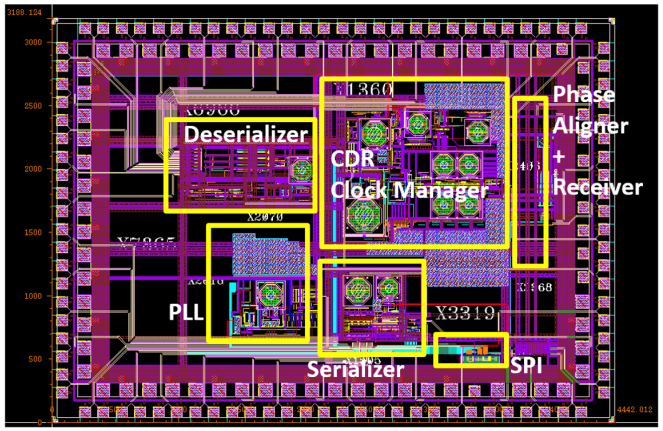
- Self-developed GBT-like prototypes verified:
  - 5.12 GHz PLL + 10.24 Gbps Serializer verified√
  - 2.56 Gbps CDR + 2.56 Gbps Deserializer verified√
  - Phase aligner under test
- 10 Gbps Laser Driver Verified √
- Customized optical module prototype Done √
- The rad-tol fiber will be investigated together with the accelerator clocking system



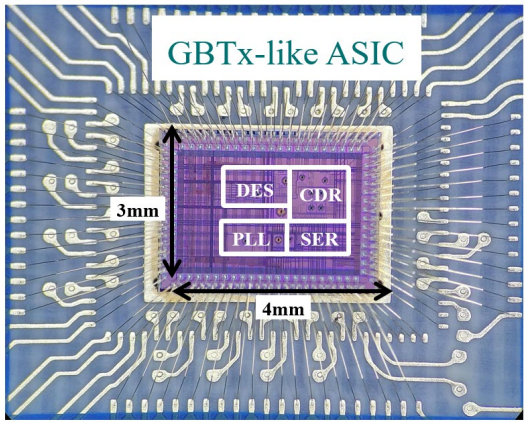
10 Gbps optical eye

Bit Rate	10Gbps	RMSJ	2.6ps
Rise Time	34.0ps	PPJ	15.3ps
Fall Time	48.9ps	Amp	589.4μW

10 Gbps optical eye diagram

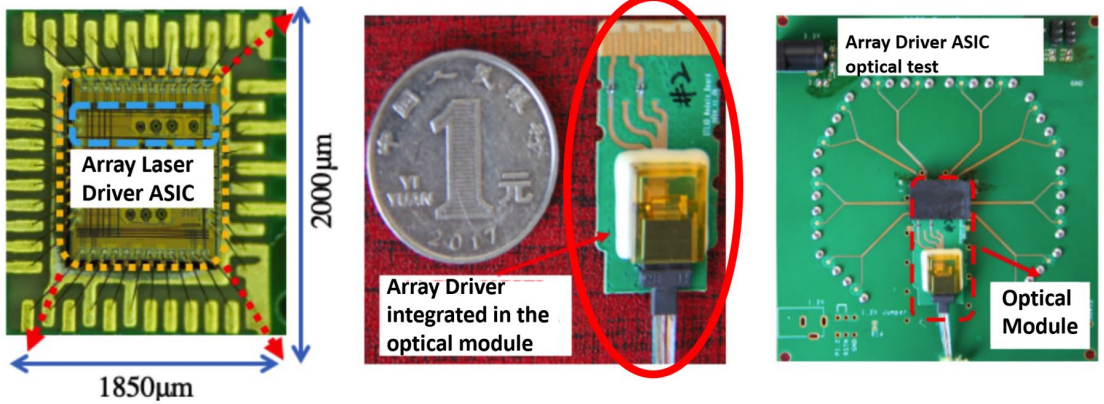


GBT-like ASIC prototype layout



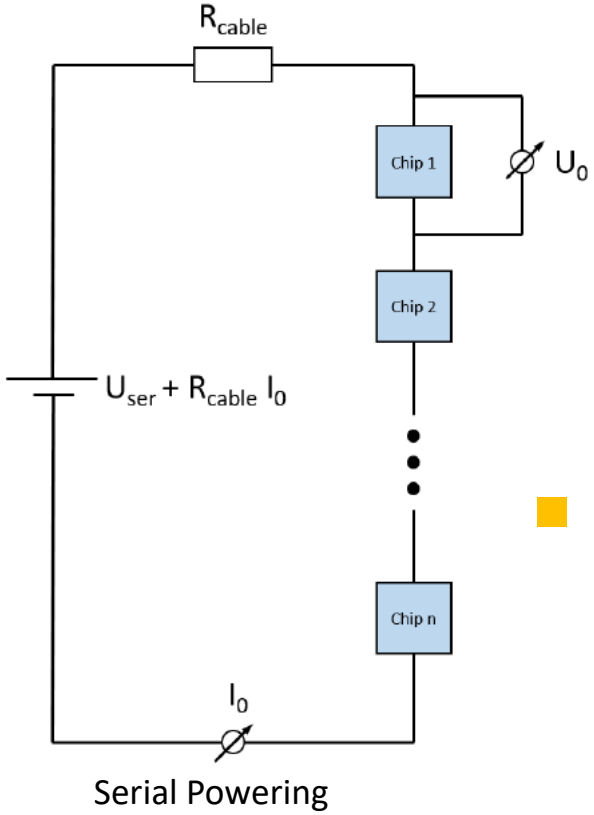
GBT-like ASIC wire-bonding picture

Customized Optical module

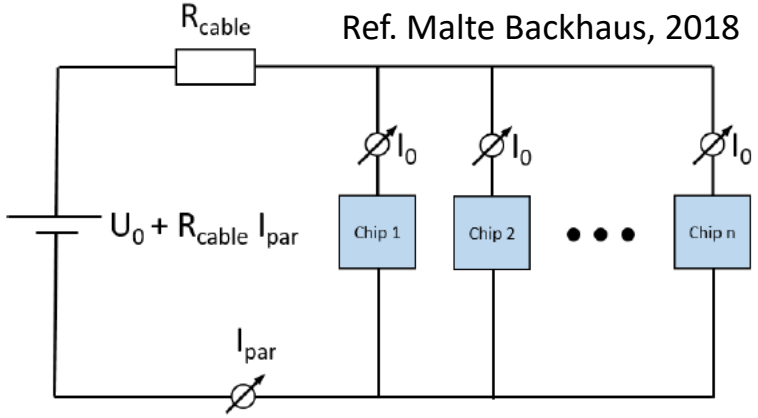


4 x 10 Gbps/ch VCSEL Array Driver with customized optical module

Technology survey and our choice on Powering



Serial Powering



Ref. Malte Backhaus, 2018

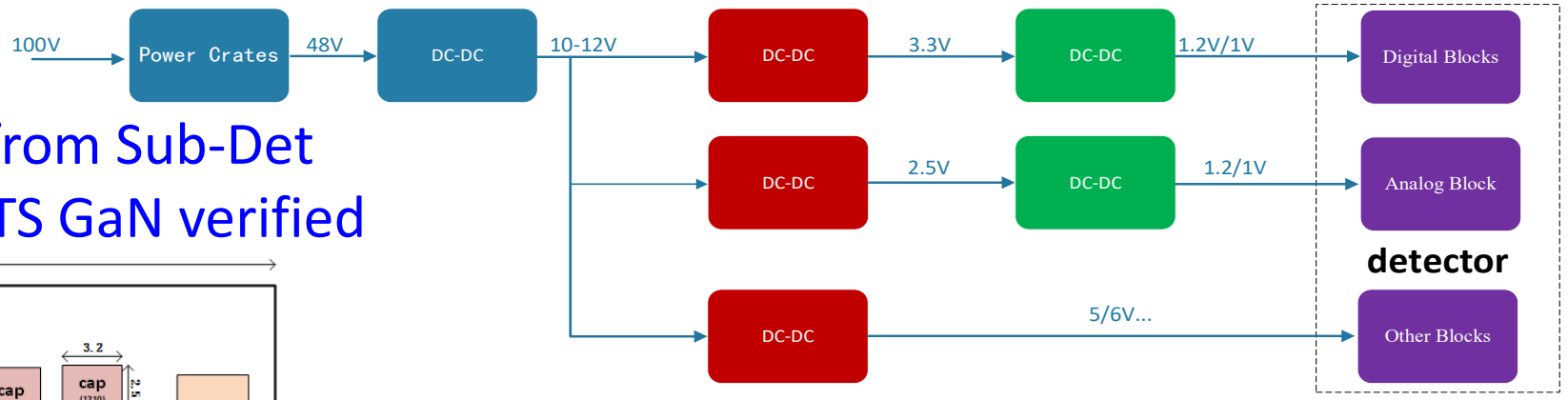
Parallel Powering

	Serial Power	Parallel Power
Material	Much less	
Cabling	Much less	
Installation	Much easier	
Maturity	New	Very mature
System Reliability	Potential issue	Very robust

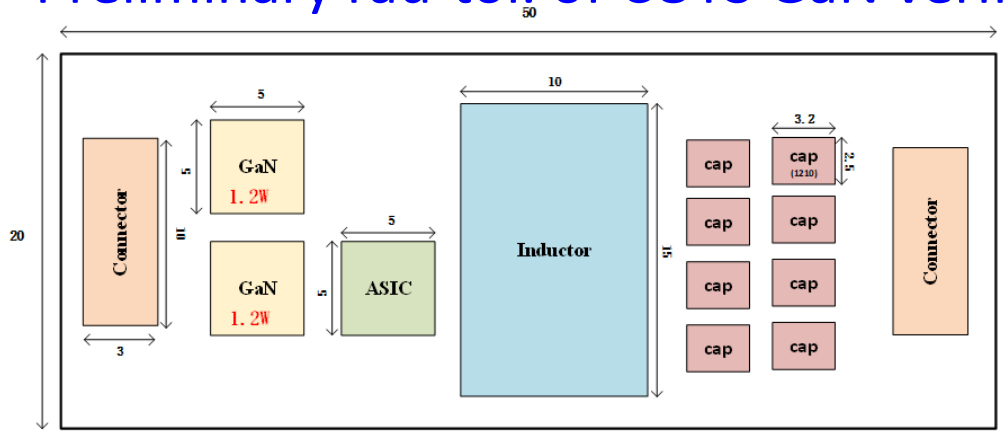
- On powering distribution
  - Serial Powering is superior in many aspects (material, cabling and installation…) than Parallel Powering, especially on VTX & TRK
  - It is also a hot area with a lot of focused R&D
  - However, due to the common substrate at negative voltage for the stitching sensor in VTX, serial powering is not feasible
- Our choice
  - As a general platform, we chose (conventional) Parallel Powering as the baseline scheme, while to keep pace on R&D of Serial Powering as the backup scheme

R&D efforts preliminary design on powering

- Structure of the power distribution system



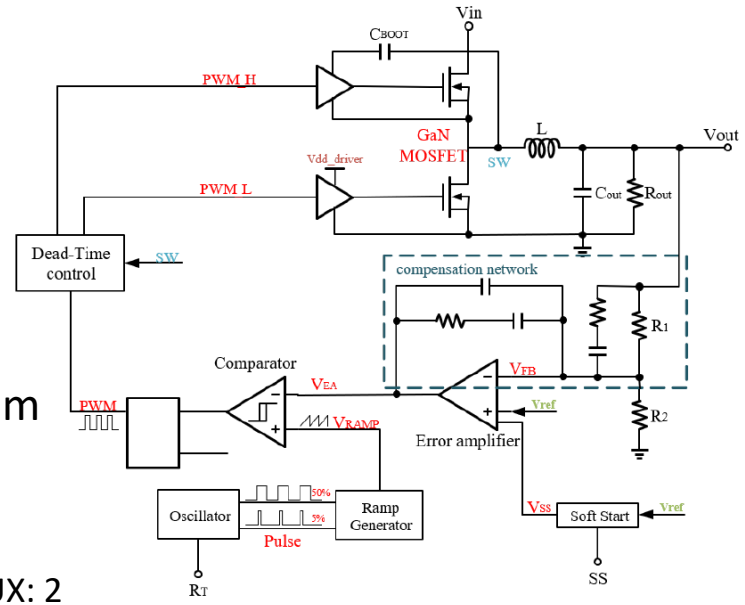
- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified



	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、3.3V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

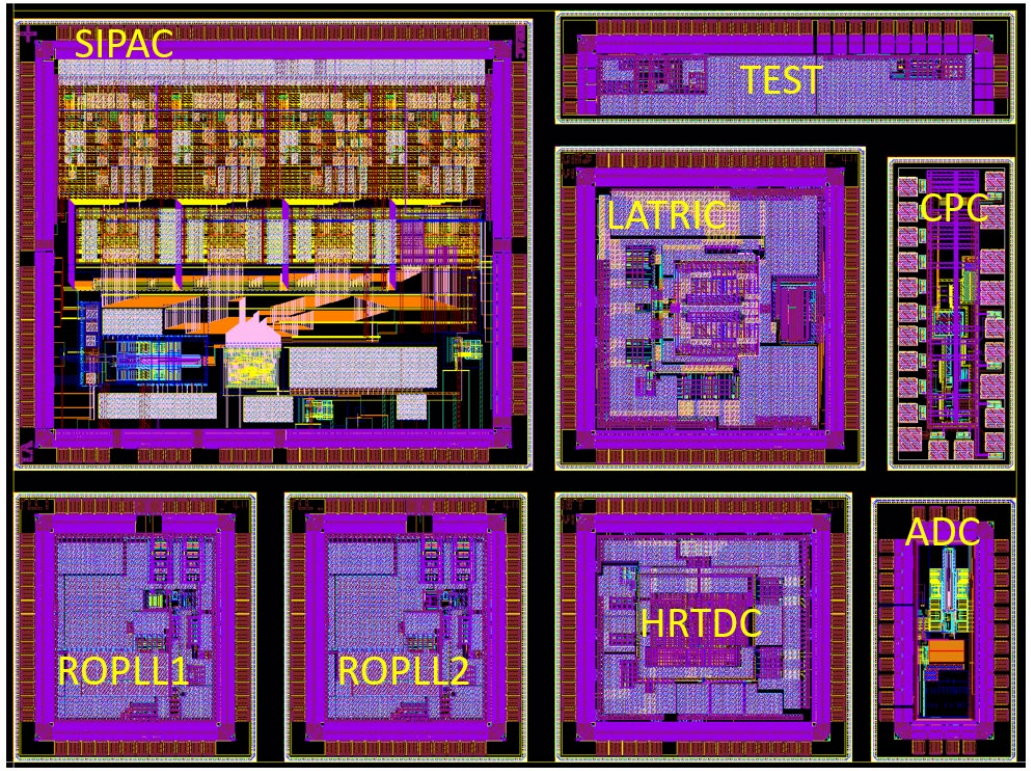
- Proposed design of BUCK DC-DC convertor

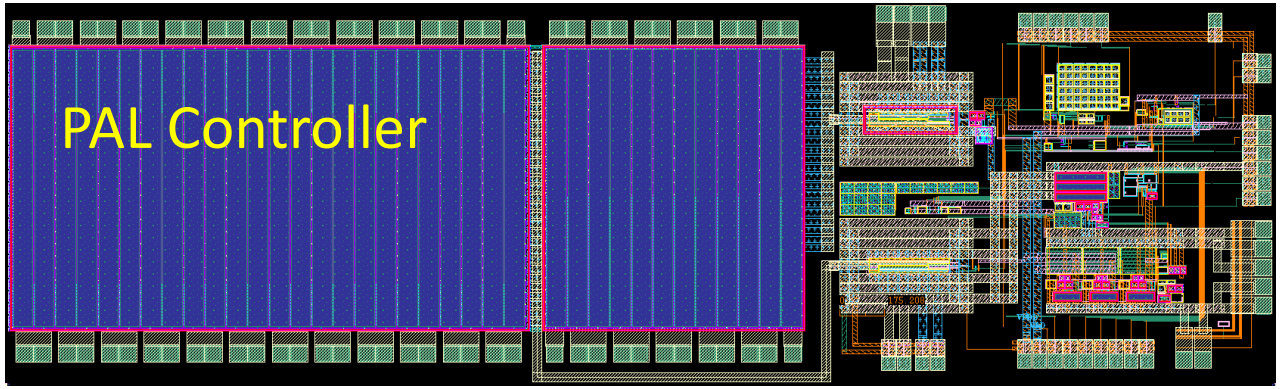
PAL Series



- Design team
  - IHEP: 3
  - NPU: 1+2
  - USTC: 1+1
  - TECHORILUX: 2

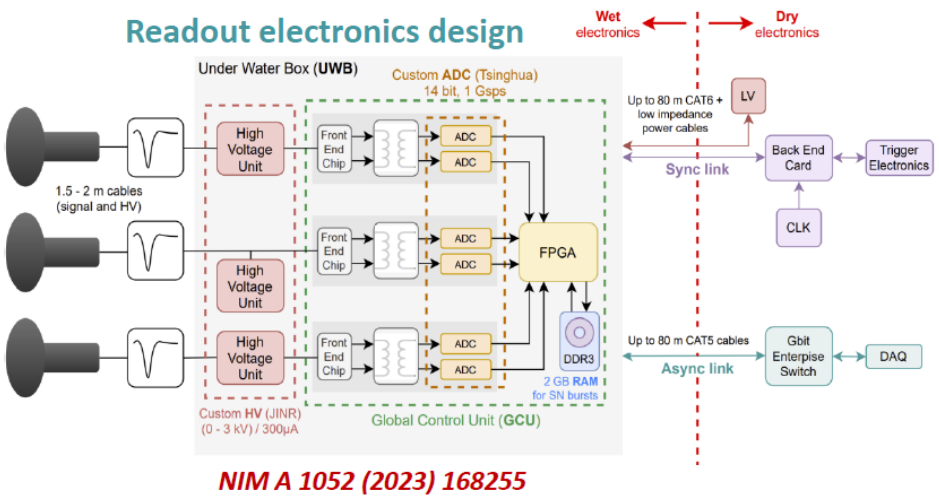
Summary of the recent tapeout

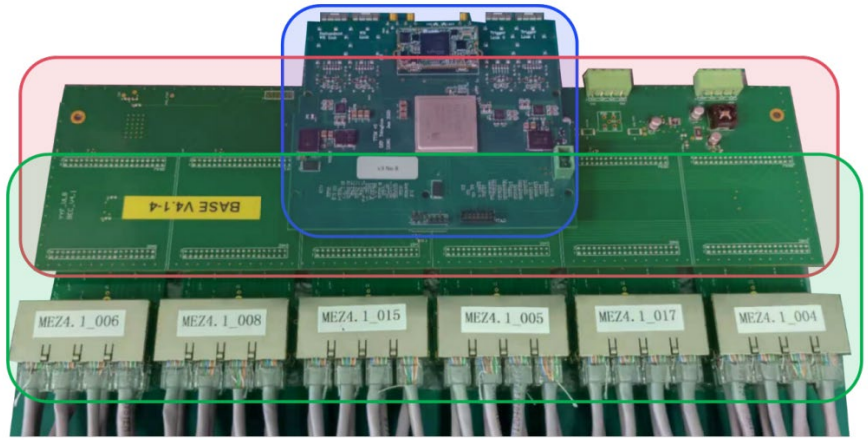




- 1st version of new ASICs (LATRIC@OTK, SIPAC@SiPM, key blocks of Data Link, ADC, TDC) has been submitted on April 7th , SMIC 55nm 4.4mm ×3.3mm
- 2nd tapeout coming in Mid July
- 1st version of PAL (DC-DC controller) also taped out on April 1st , SMIC 180nm 40V-HV

Related R&D and experience on BEE



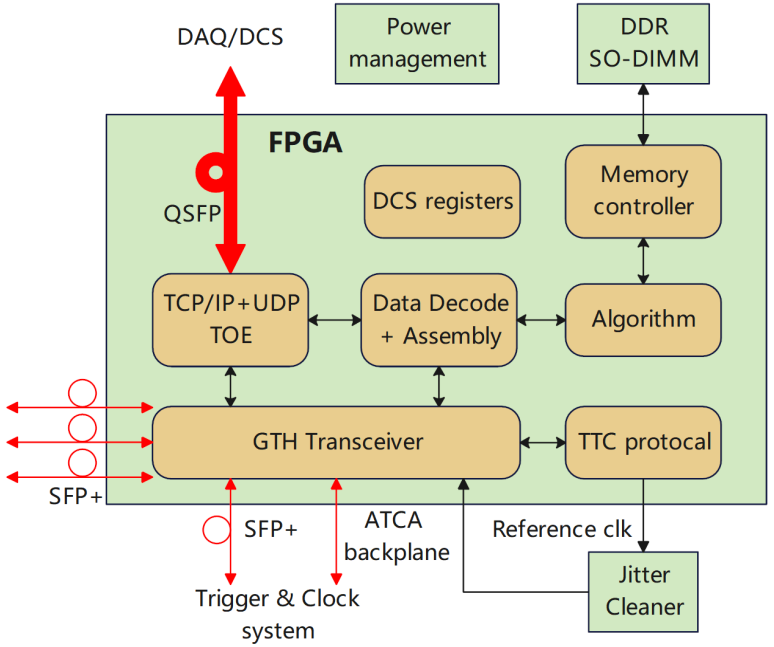


The back-end box for the JUNO experiment

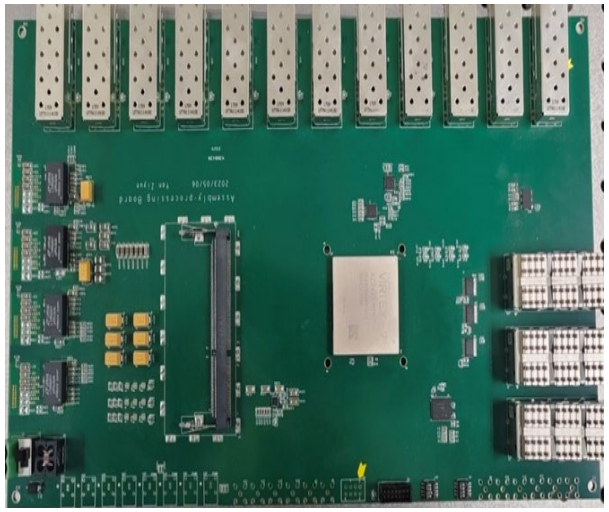
- located between trigger system and front-end electronics,
- Collects the incoming trigger request for trigger system,
- Fanout the synchronized clock and the trigger decisions to front-end electronics.

- Red box: The base board provides the power supply,
- Blue box: Trigger and Time Interface Mezzanine (TTIM) with WR node,
- Green box: The extenders interface with ethernet cables coming from underwater front-end boxes.

Detailed design on common BEE



The back-end Card structure



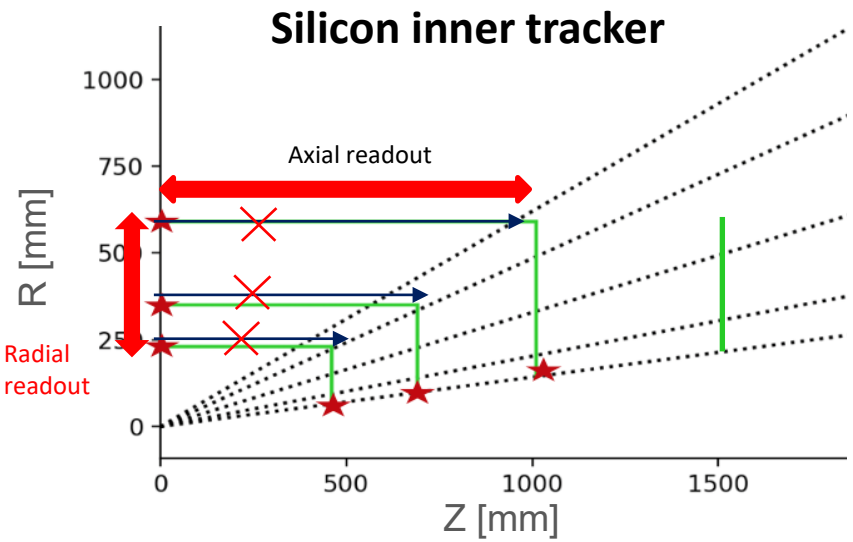
Data aggregation and processing board Prototype for Vertex detector

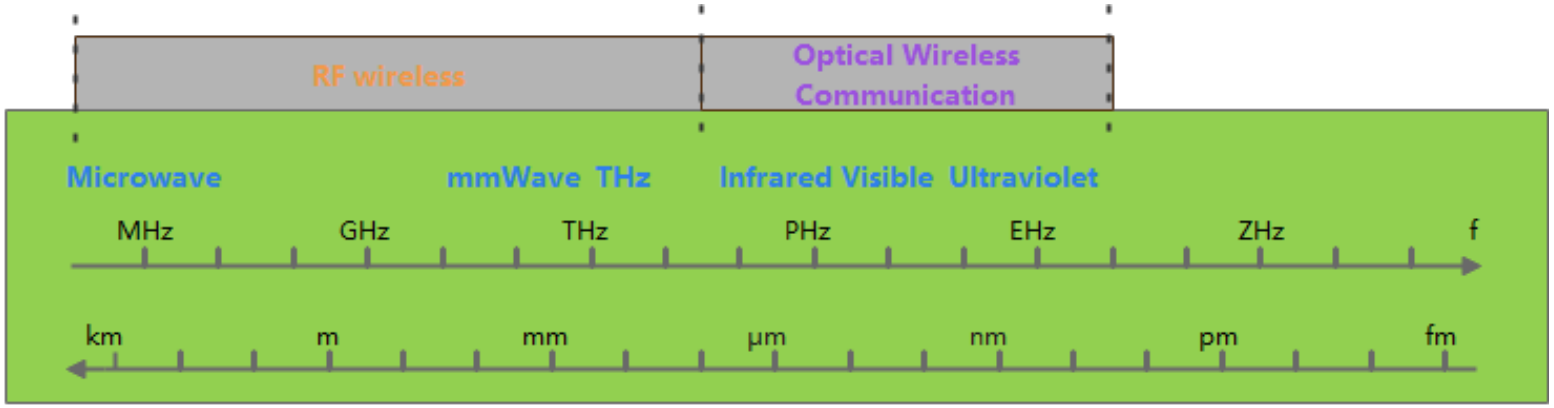
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between the optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- A cost-driven device selection: FPGA XC7VX690T
- Interface： SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Alternative scheme based on wireless communication





- Radial readout with mm-wave
  - 12- 24 cm transmission distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz， 45GHz， 60GHz， 77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

- Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme
- Three major solutions were investigated through R&D, two were selected with corresponding schemes
- R&D people-power in parallel with the main R&D

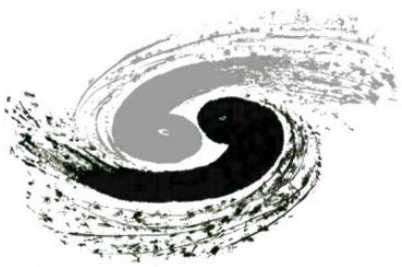
On-detetor interface defined

Detector	Max data rate per fiber (Gbps)	Fibers per module	Fiber sum	BEE sum	Data crate sum	Module Max Power (W)	Total Power (kW)	Power channels	Power crate sum	HV requirements	HV channels sum	HV crates sum
VTX	8	1~2	88	6	1	25	0.45	66	2	~-10V	66	1
TPC	0.1	1	496	32	4	32.2	16	496	6	-500V	496	4
ITK-Barrel	0.96	1	2376	149	15	11.2	26.6	2376	25	50~200V	2376	10
ITK-EndCap	2.2	1	1236	78	8	11.2	13.8	1236	2	50~200V	1236	8
OTK-Barrel	1.4	1	880	34	4	27.6	195	2640	55	150~200V	880	4
OTK-EndCap	0.7	1	544	45	6	27.6	60	1632	34	150~200V	544	4
ECAL-Barrel	4.8	4 (2)	1920	60	6	31	17.5	480	5	40~60V	480	2
ECAL-EndCap	4.8	4 (2)	896	28	4	31	9.5	224	4	40~60V	224	2
HCAL-Barrel	0.14	1	5536	346	36	9	66.1	5536	58	40~60V	5536	26
HCAL-EndCap	1.75	1	3072	192	20	11	41.3	3072	32	40~60V	3072	14
Muon-Barrel	0.004	1	288	18	2	2.6	0.76	288	3	40~60V	288	2
Muon-EndCap	0.01	1	96	6	1	4.7	0.45	96	1	40~60V	96	1
Sum			17428	994	107		447.46	18142	227		15294	78

Only FEE Power summarized in the table. Extra power for BEE & crate efficiency will be considered in the mechanical system for the counting room

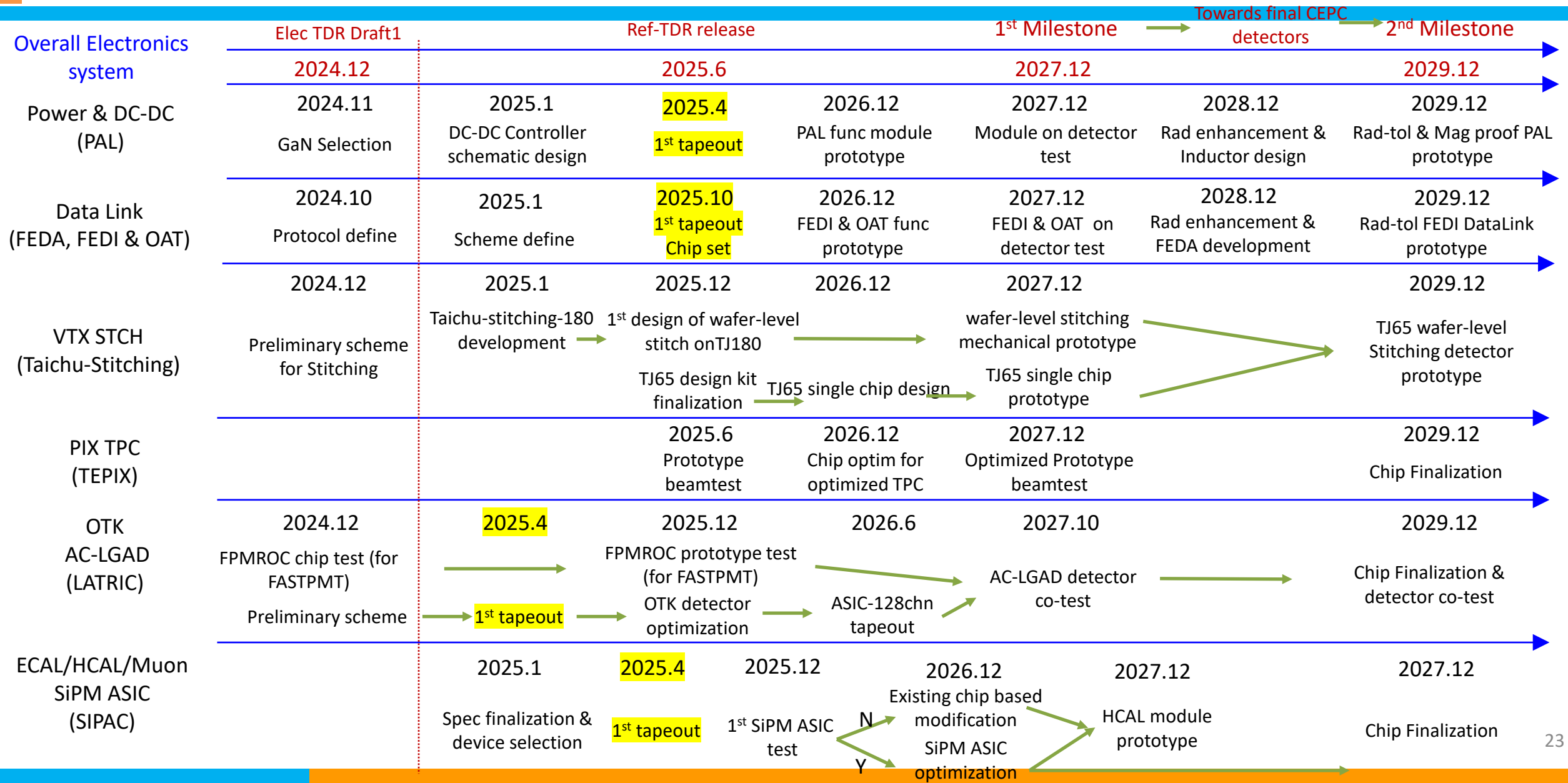
Research Team

- A wide collaboration was built involving most of the affiliations in the HEP field in China (~50 people involved in different areas).
- We are working to expand the collaboration, including attracting international colleagues. We are also trying to join in the DRD7.



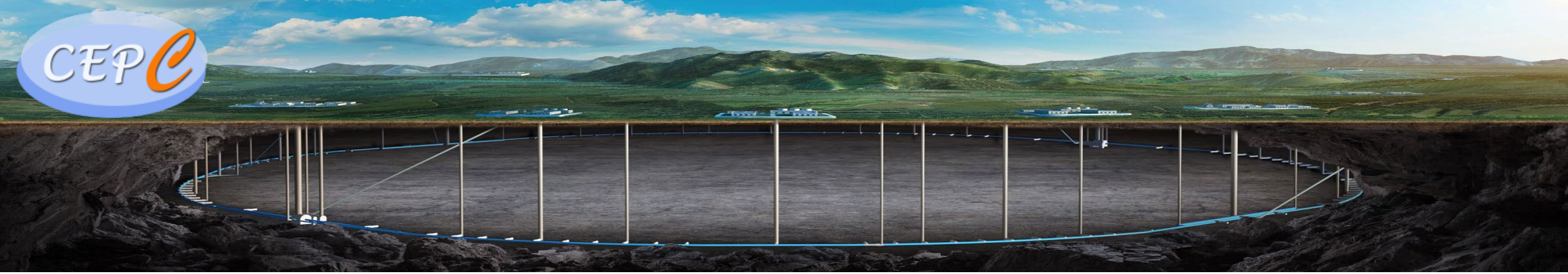

- Overall electronics and BEE: IHEP(5)
- Sub-detector readout electronics: IHEP(11), Tsinghua(5), CCNU(3), NPU(7), SDU(4), NJU(3)
- Data link: CCNU(3), IHEP(3), USTC(2), NPU(4)
- Powering: NPU(3), IHEP(2), USTC(2)

Timeline for all the FE ASICs – common ASIC – long term



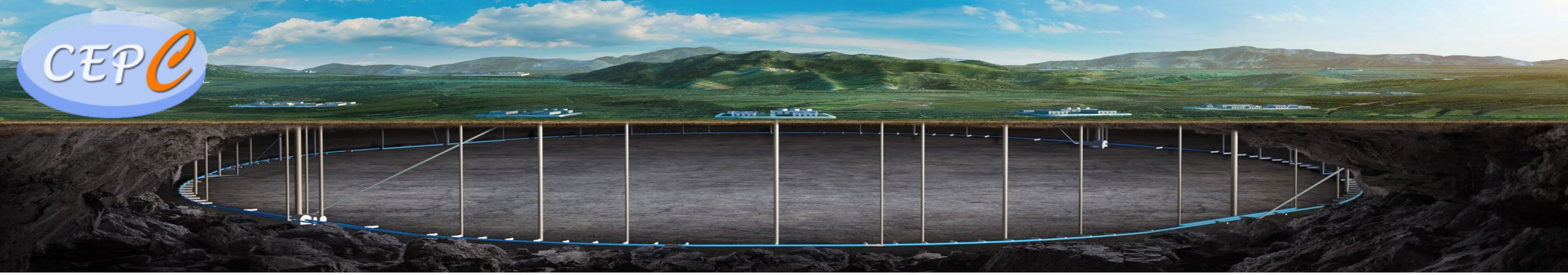
Summary

- Full Data Transmission (Frontend Triggerless) + Backend Trigger was chosen to be baseline for the 1st ten-year
  - Background rate under ctrl for Higgs & Low Lumi Z
  - Backup scheme on Partial full data transmission + Partial fast trigger (VTX only if necessary)
- All ASIC design with dedicated people power, 1st ver. of key ASIC already taped out
  - 3-year to prototype the ASIC
  - 5-year to be finalization
- No show stopper is found for the electronics framework & the Sub-Det readout.
- Key R&D to be kept on pace
  - Serial powering for future silicon detector
  - Wireless comm as an alternative scheme, while parallel people power allocated other than the main R&D



Thank you for your attention!

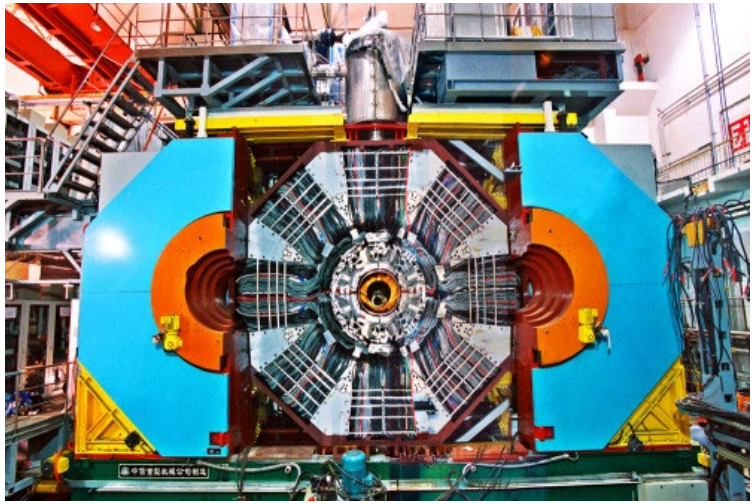
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences



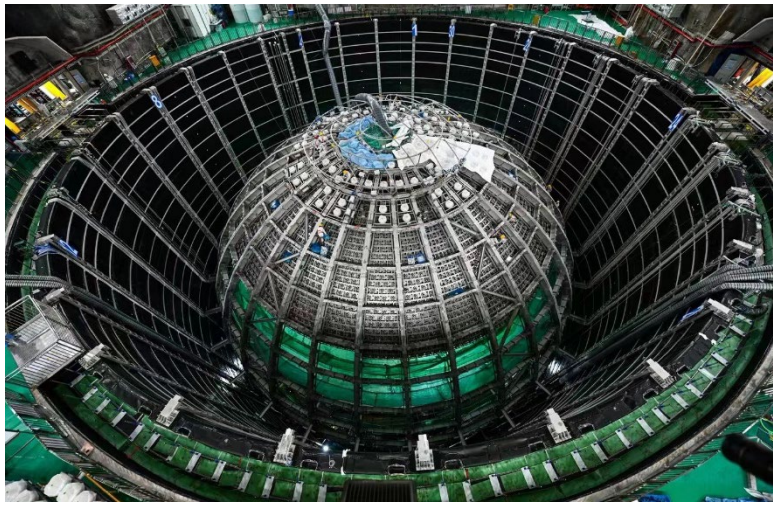
BACKUP - ASIC

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

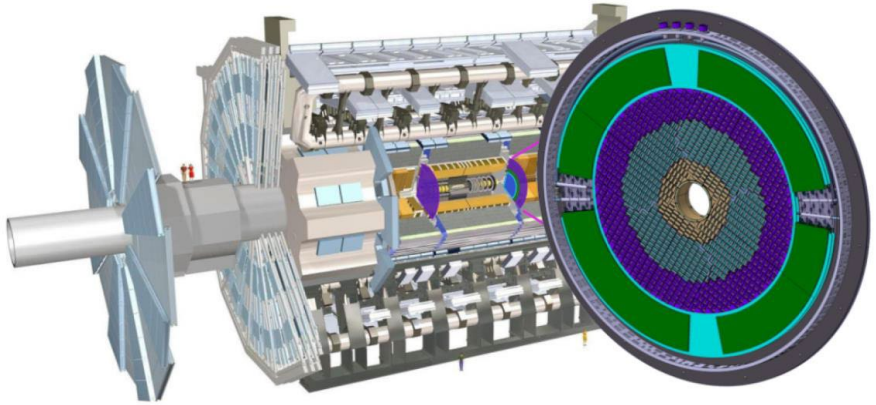
Previous experience on electronics system



BESIII

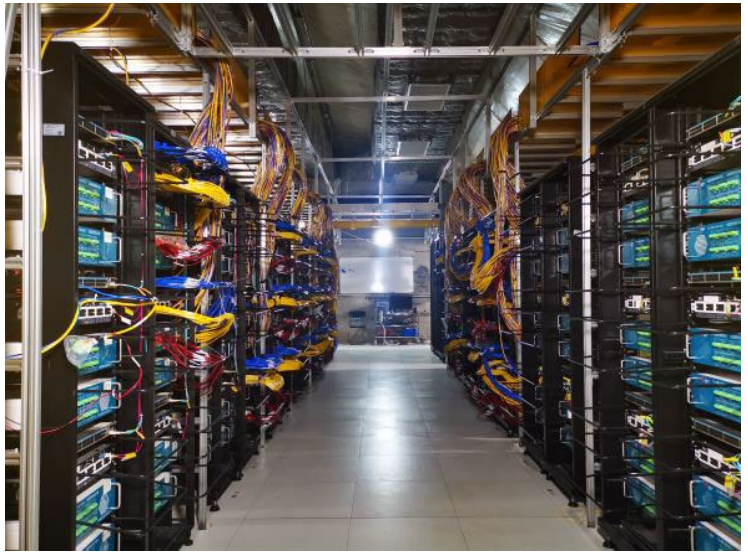


JUNO experiment



ATLAS HGTD
(Ref. J. Zhang http://b.mtw.so/6ide9O)

- Our team has developed the electronics systems for most of the major particle physics experiments in China, including BESIII, Dayabay, JUNO, LHAASO…
- Also in international collaborations as ATLAS HGTD…
- We have extensive experience in electronics system design from the FEE to BEE



Status of FE & common ASIC

Name	Application	Functional	Maturity	Comment	Similar chips
FEDI	Common Elec	Data Link	2~3	Key blocks ready, protocol TBD	lpGBT
OAT	Common Elec	Optical	3~4	Real module verified	VTRx
FEDA	Common Elec	Data Aggregation	2	Although needs scheme, but a pure digital ASIC, low risk	GBTx、HCC
PAL	Common Elec	DC-DC	2	Initial stage, but the scheme are conventional and low risk. GaN has been preliminarily verified. Inductors to be selected and tested for Magnet.	bPolx，FEAST
Taichu	VTX	VTX-Stitching	2~3	Single chip fully verified. Will be focused on stitching issues	ALICE-ITS3
TEPIX-TPC	TPC	Pixel TPC	3~4	TPC module to be beam-tested. Further optimization is ongoing	Gridpix（Timepix3）
COFFEE	ITK	HVCMOS	3	ITK HVCMOS pixel sensor chip, three versions verified.	LF-MONOPIX
LATRIC	OTK	LGAD-TOF	2	With preliminary scheme, while TDC & similar FE is already tapedout and wait for test. Cd & power to be optimized for a real design.	ALTIROC
SIPAC	SiPM ASIC	ECAL, HCAL, Muon	2~3	Schemes verified in previous chips. No show stopper for all key blocks. Waiting for the detector finalization & device selection to start the design	HGCROC、SPIROC

Maturity: 1： from scratch; 2: initial design proposed, R&D needed; 3: with experience or previous design, no show stopper; 4：prototyped, further optimization required; 5： verified for the real detector.

People-power for Electronics system

	Overall	BEE	VTX	TPC	ITK+OTK (LATRIC)	CAL (SiPM)	Muon	Data Link	Power	Wireless
Staff	5	1	10	1	9	5	1	9	7	4
Postdoc + Student	0	3	8	4	10	6	0	16	3	5
Total Sum	5	4	18	5	19	11	1	25	10	9

- The headcounts are not to the FTE
- Some staffs are shared by multiple projects, while postdocs / students are dedicated to the projects

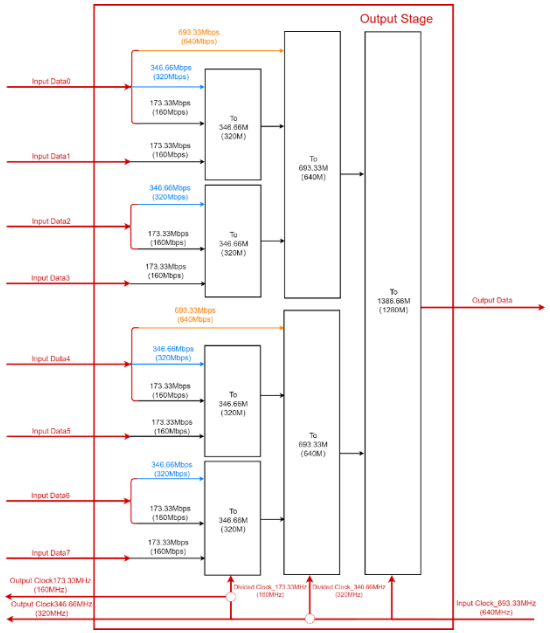
Affiliations for Electronics system

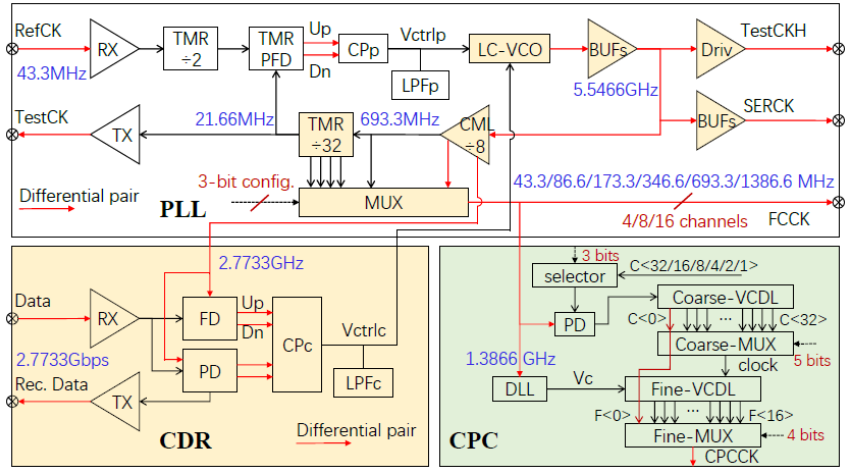
	Overall	BEE	VTX	TPC	ITK+OTK (LATRIC)	CAL (SiPM)	Muon	Data Link	Power	Wireless
IHEP	×	×	×		×	×	×	×	×	×
CCNU			×		×	×		×		
THU				×						
NPU			×					×	×	
NJU			×		×			×		
USTC								×	×	
WTU					×			×		
IPAS								×		
HPU					×			×		
T-ORILUX									×	
SDU			×							
NCU			×							
IME										×
USST							×			

Naming of new ASICs

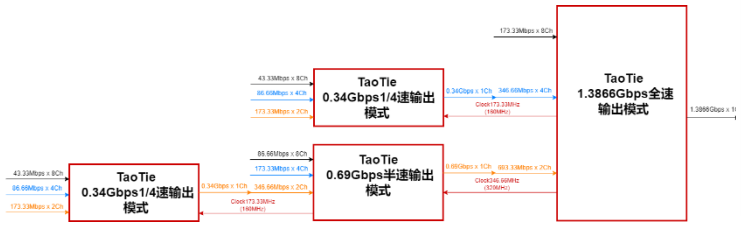
- Data Link：
  - FEDA: Front-End Data Aggregator ASIC
  - FEDI: Front-End Data Interface ASIC
  - OAT： Optical Array Transceiver Module
    - ALDD: Array Laser Diode Driver ASIC
    - ATIA: Array Transimpedance Amplifier ASIC
- Power：
  - PAL: Power At Load
- OTK ASIC:
  - LATRIC： LGAD Timing and Readout Integrated Chip
- SiPM ASIC：
  - SIPAC： SiPM ASIC for Calorimeter

Current status of the Data Link chip set

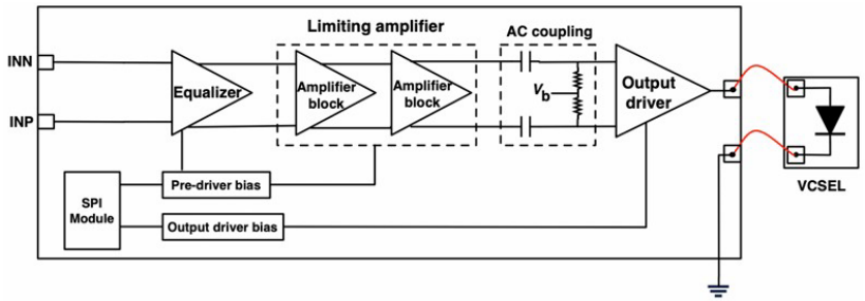




FEDI clock system



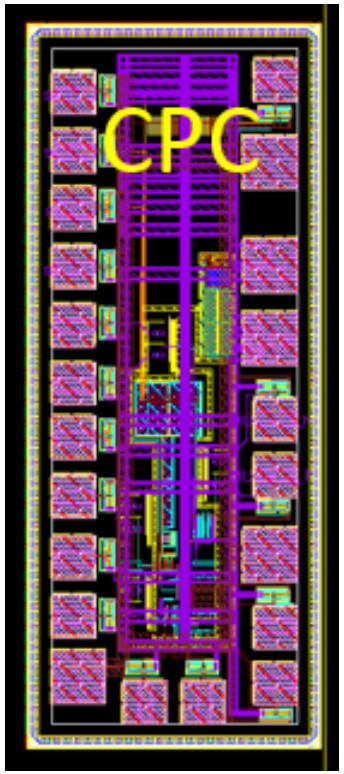
FEDA

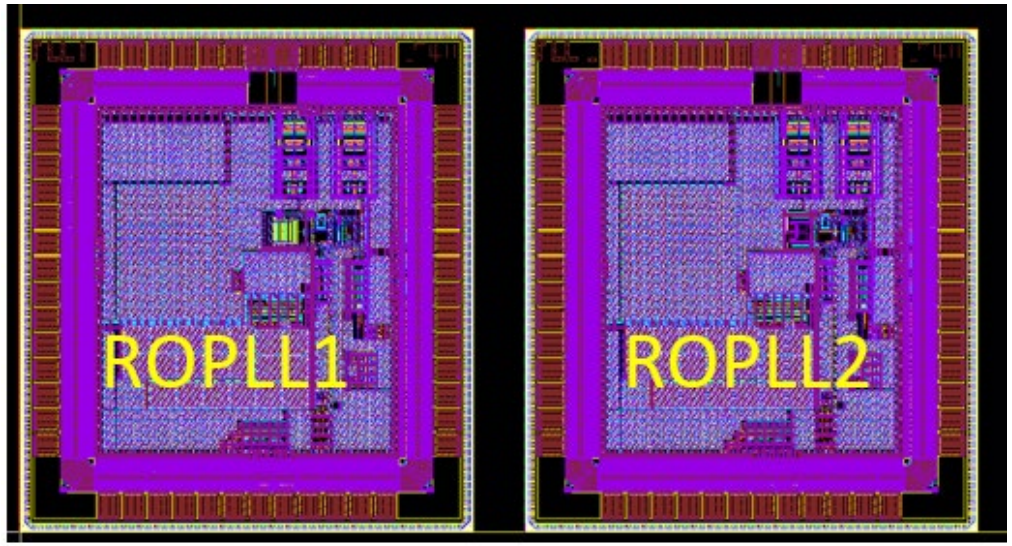


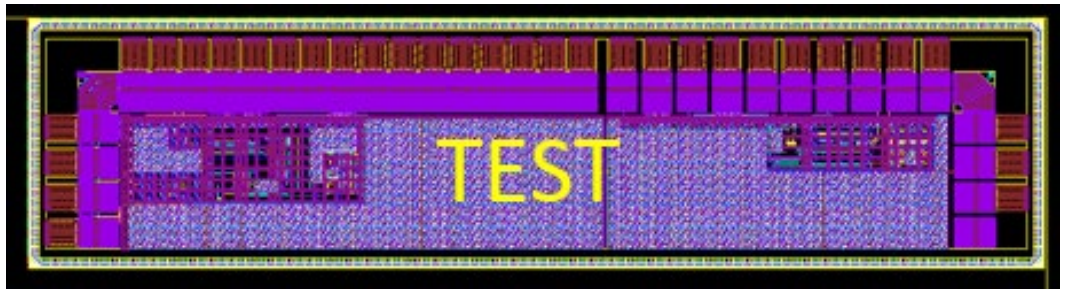
OAT VCSEL Driver

- Main schemes established (details skipped)
- Most new design proceeded to the code level with block simulation
- Design Team (not FTE)
  - IHEP:3 staffs +3 students
  - CCNU:2+8
  - NPU:2+2
  - USTC:1+2
  - WTU:2+2
  - IPAS:1+1
  - HPU:1+2

Tapeout status of the Data Link chip set

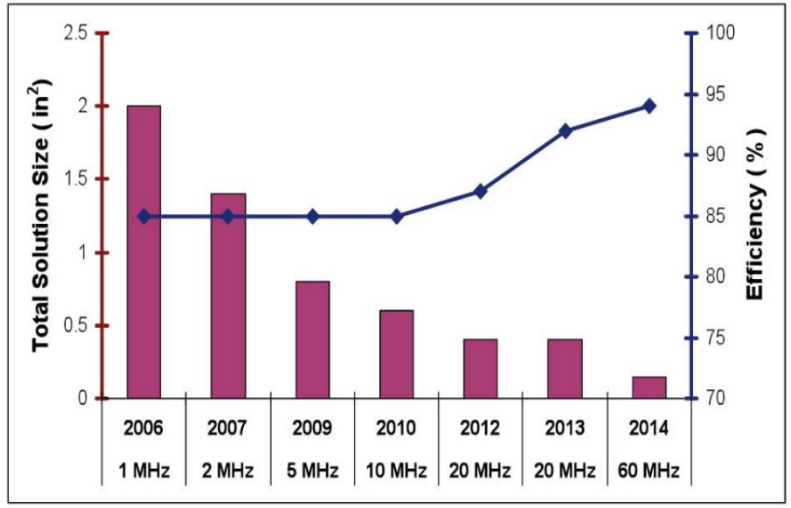




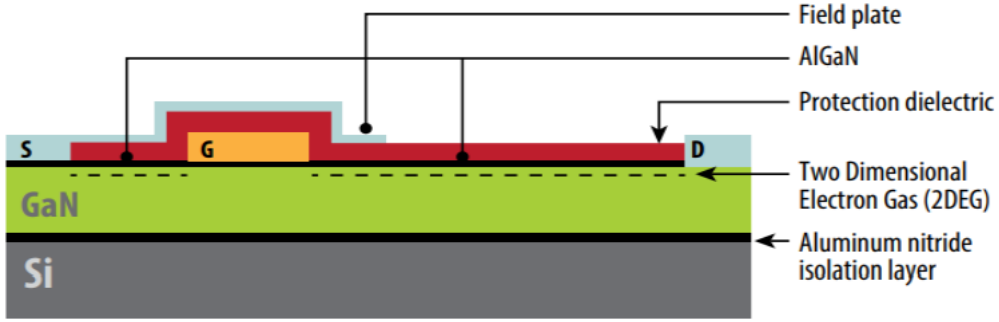


- Some new blocks submitted for verified on April 7th
- The full chip set aiming to tapeout in July or October 2025

Technology survey and our choice on Powering

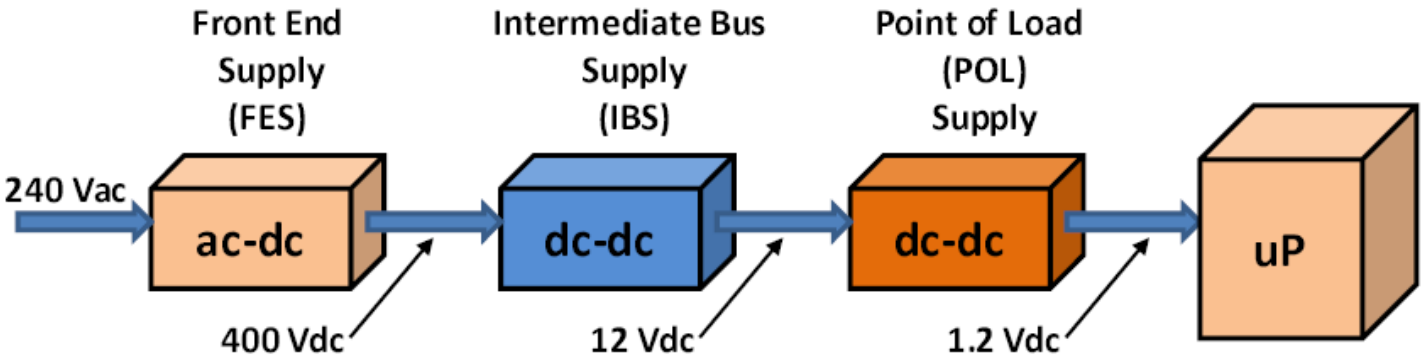


Higher switching Freq, smaller size,
higher efficiency, lower on-resistance



Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

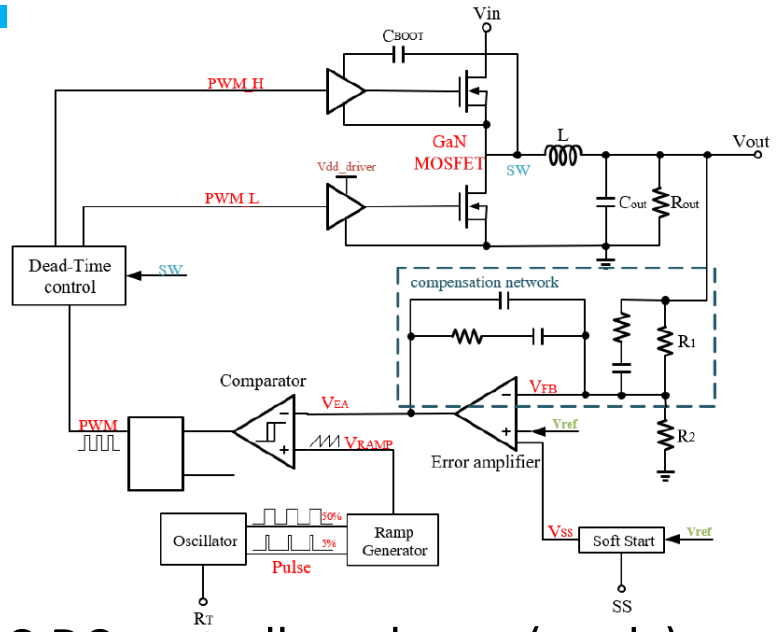
Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency



A 400V to 1.2V chain, lower power loss on cable

- Investigation was also conducted to compare the key component schemes of the power module, esp on LDO & DC-DC convertor.
- The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.
- We choose a GaN-based DC-DC as the baseline power module scheme. This also enables high voltage power distribution, for low cable material and low power loss.

Current status of the PAL Power module



DC-DC controller scheme (ready)

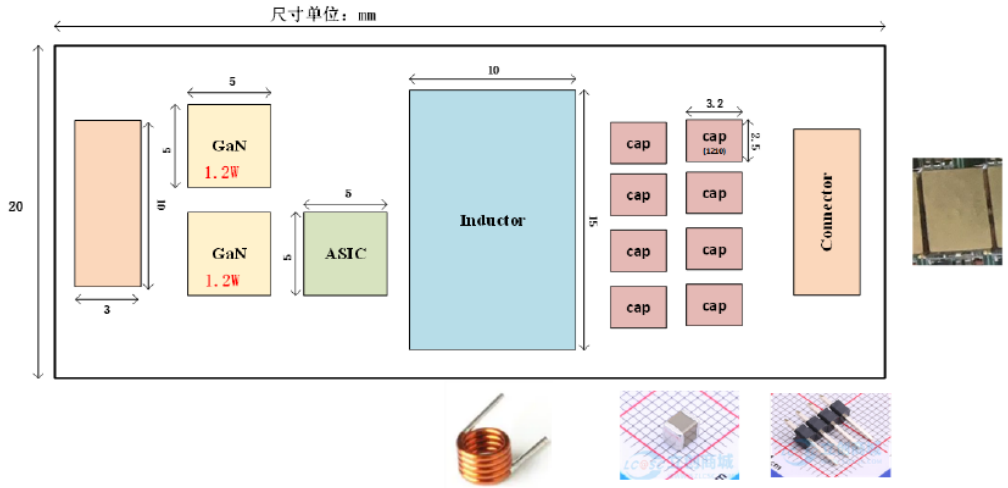
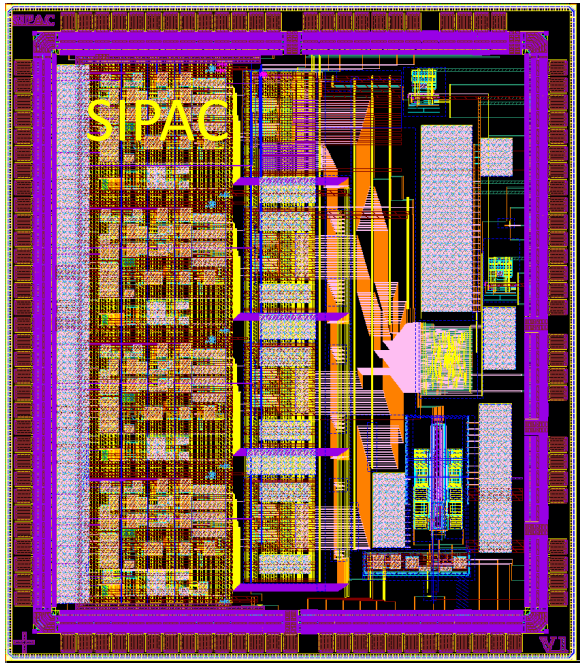
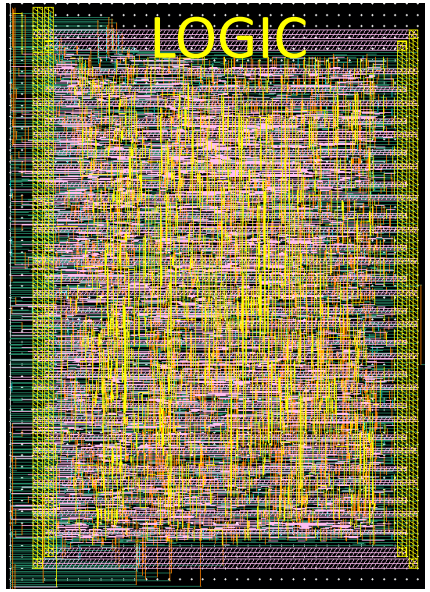


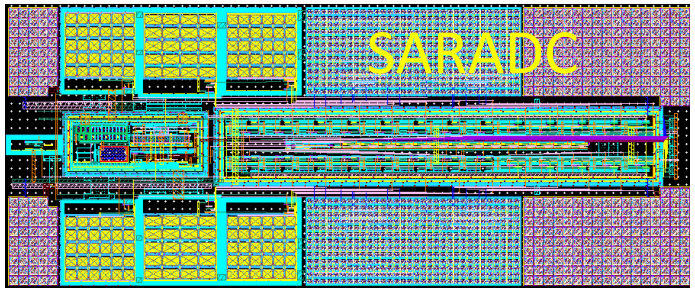
Figure 11.61: Floor plan of Basha DC-DC module

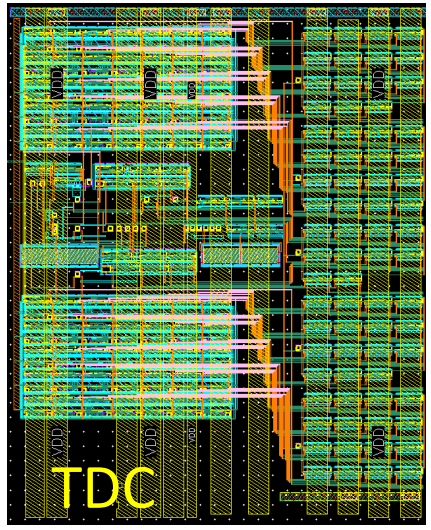
- Chip design:
  - The kernel GaN transistor selected by rad-test
  - DC-DC controller 1st tapeout in April
- Module design
  - Scheme defined to be 48V→12V，12V→1.2/3.3
  - Experienced design team from Univ. & Industry contacted and will be involved very soon
- Air Core Inductor study
  - Main constraint for the module size
  - Try to investigate with industrial help
- Commercial DC-DC & LDO
  - By TID test, some COTS power device found that can even survive at CEPC level
  - Can be backup devices at early stage for prototypes
- Design team
  - IHEP: 3
  - NPU: 1+2
  - USTC: 1+1
  - TECHORILUX: 2

Tapeout status of the SIPAC chip





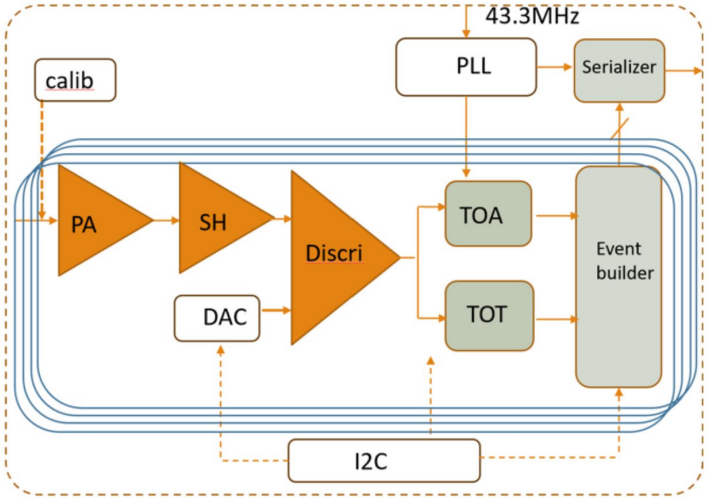




- 1st version MPW in April aiming for the main functionality and analog performance
- 4CH analog, TDC, ADC, central logic included in this version
- ADC@SAR has also been verified as a single chip

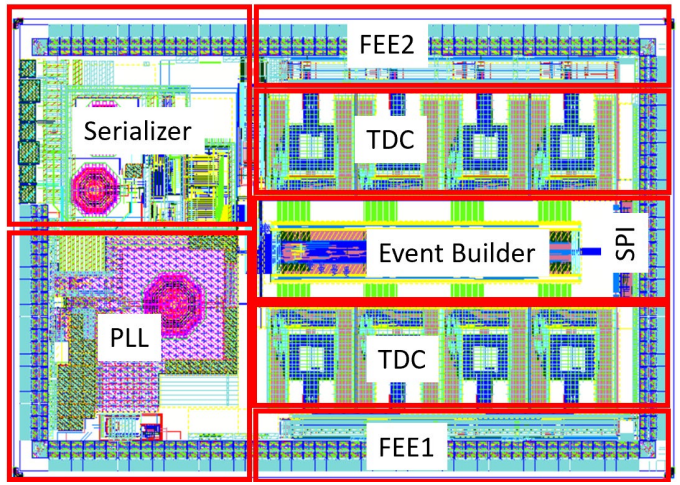
36

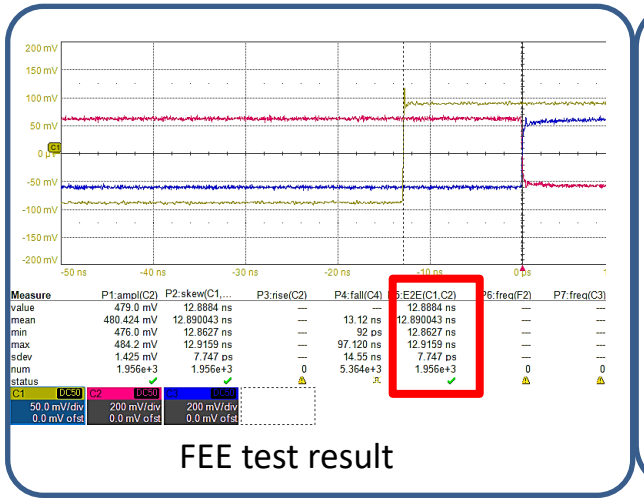
Current status of the LATRIC ASIC for OTK



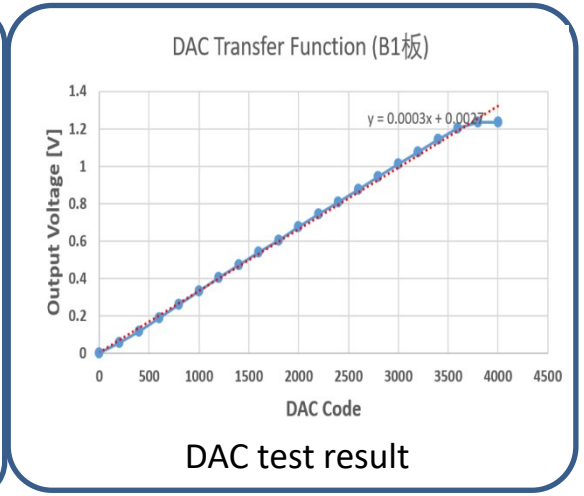
LATRIC diagram

- LATRIC scheme proposed according to current OTK design (for Ref-TDR)
  - Waiting for the new LGAD prototype for further optim.
  - 1st tapeout in April
- For the co-test at early stage, FPMROC (for TOF-PET) has been tapeout and tested with 10ps spec
  - Key analog blocks with similar scheme as LATRIC, power will be optimized for 30ps spec
  - TDC scheme will be replaced by a low-power version





FEE test result

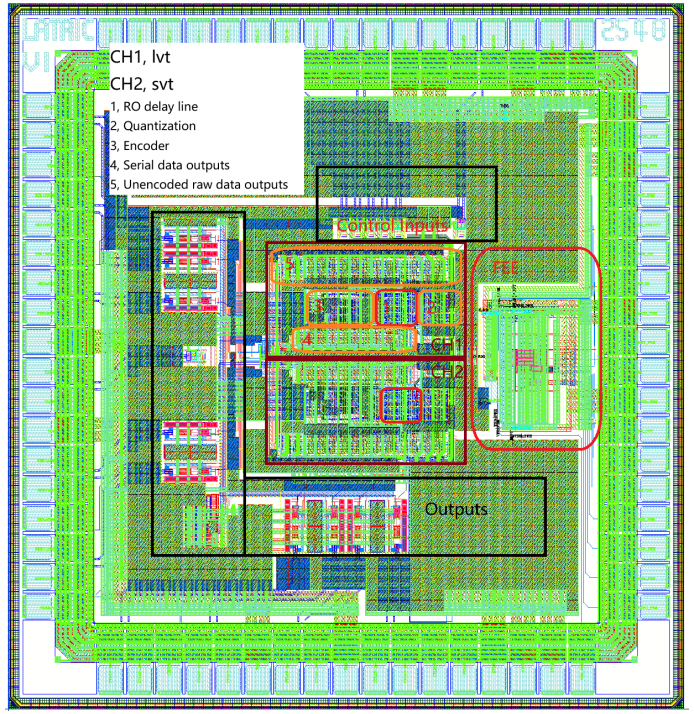


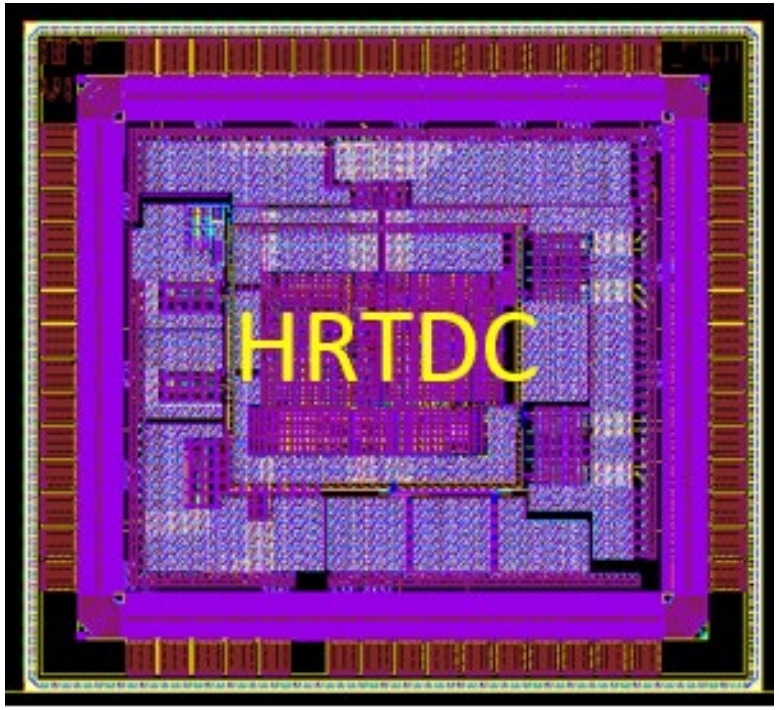
DAC test result

FPMROC 1st tapeout

- **Design team**
  - **IHEP: 3+2**
  - **CCNU: 2+3**
  - **WTU: 1+1**
  - **HPU: 1**

Tapeout status of the SIPAC chip





- 1st version MPW on April 7th aiming for the main functionality and the full signal chain
- FEE + TDC + Serializer integrated
- A high resolution TDC design also submitted for verification

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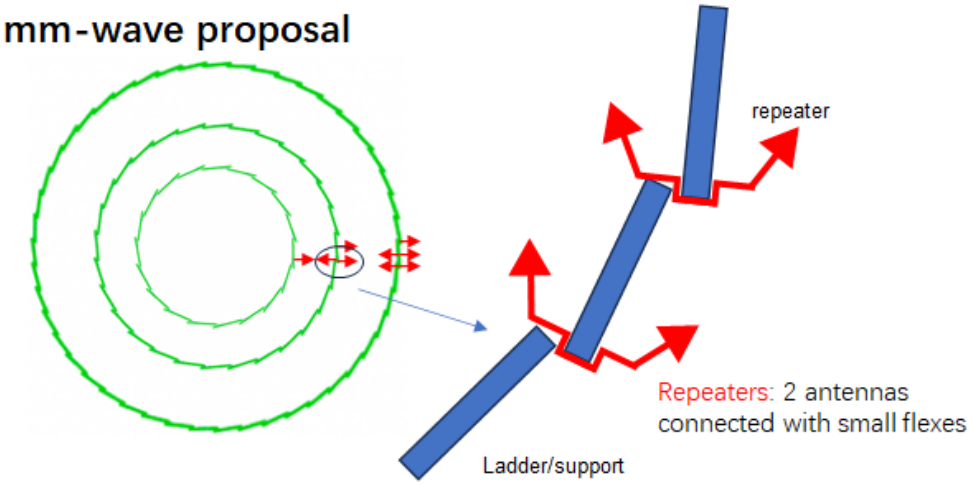
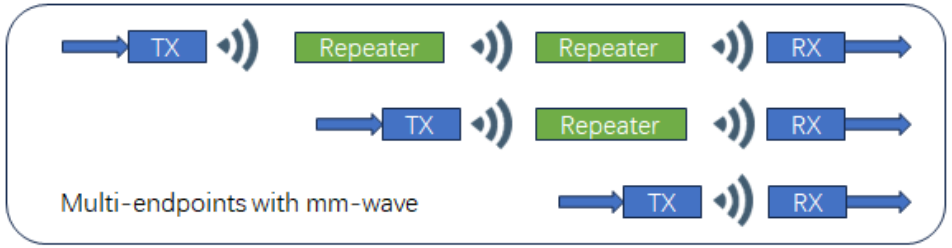
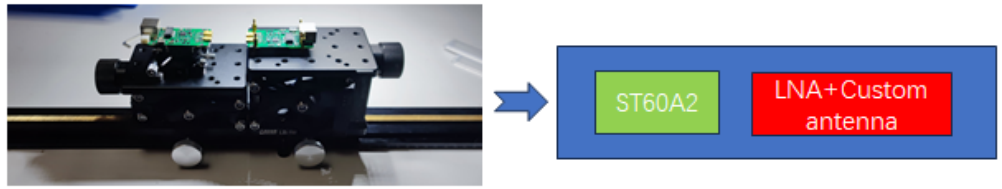
R&D efforts and results on WLess Comm

mm-wave proposal





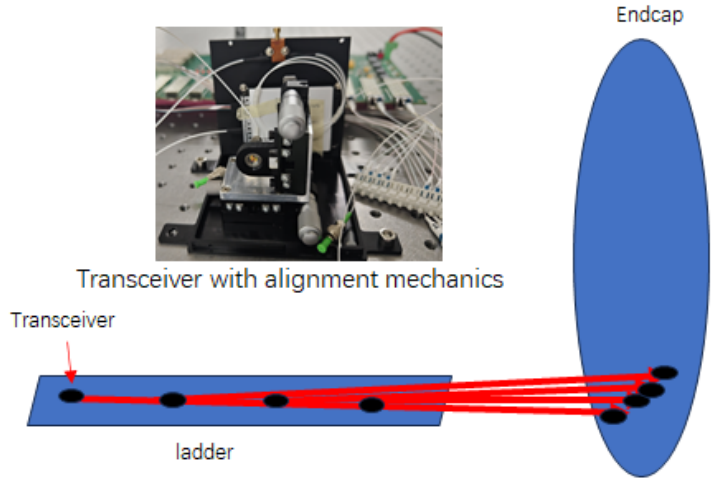


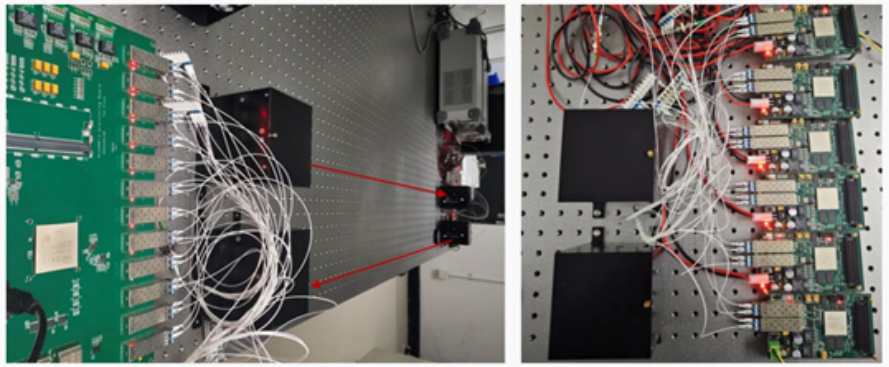
Test with evaluation boards – SK202

- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

Optical wireless proposal



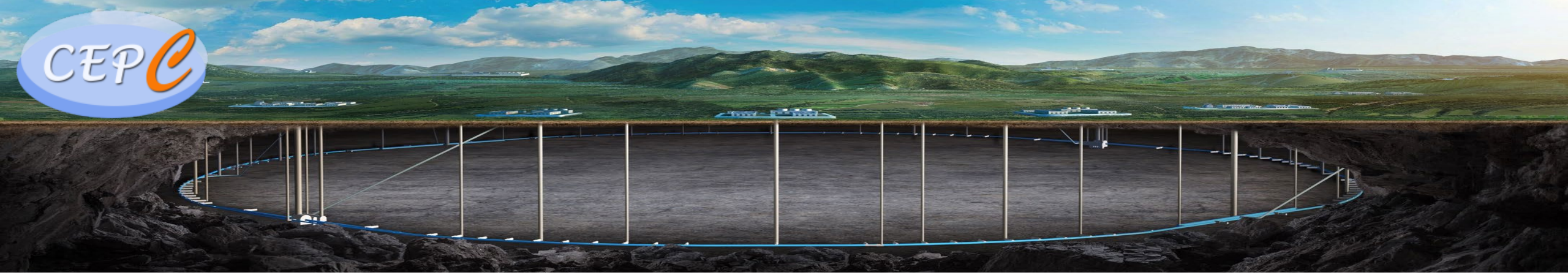


DWDM transceivers +AWG + lens

- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

A summary of FEE power

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 800mW/chip	20mW/chn 2.56W/chip		280μW/chn 35mW/chip 100mW/cm^2	15mW/chn 240mW/chip				
Max chips@module	29	14	14	22	22	1115	64	120	8	92	167
Power@module (W)	5.8	11.2	11.2	27.6	27.6	32.2	30	30	9	11	4.7

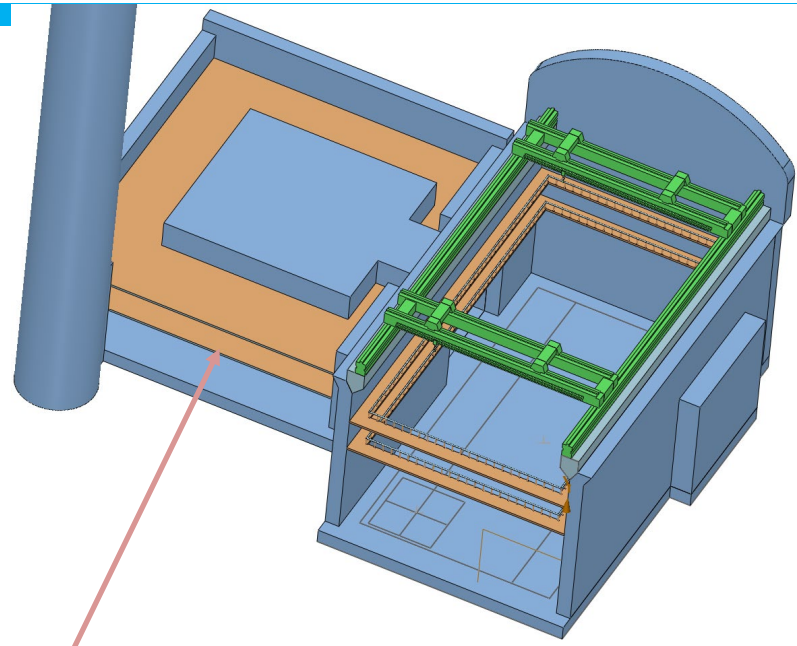


BACKUP – Counting room

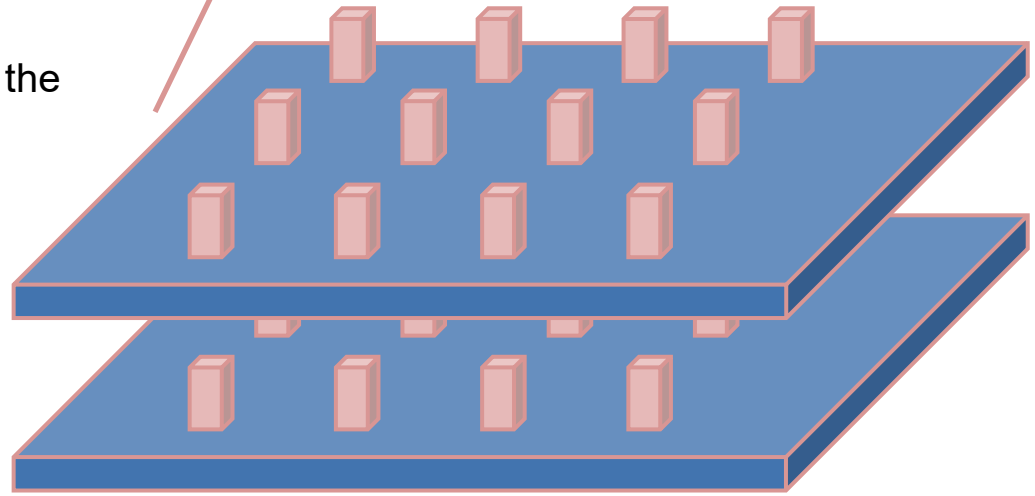
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Electronics in the counting room

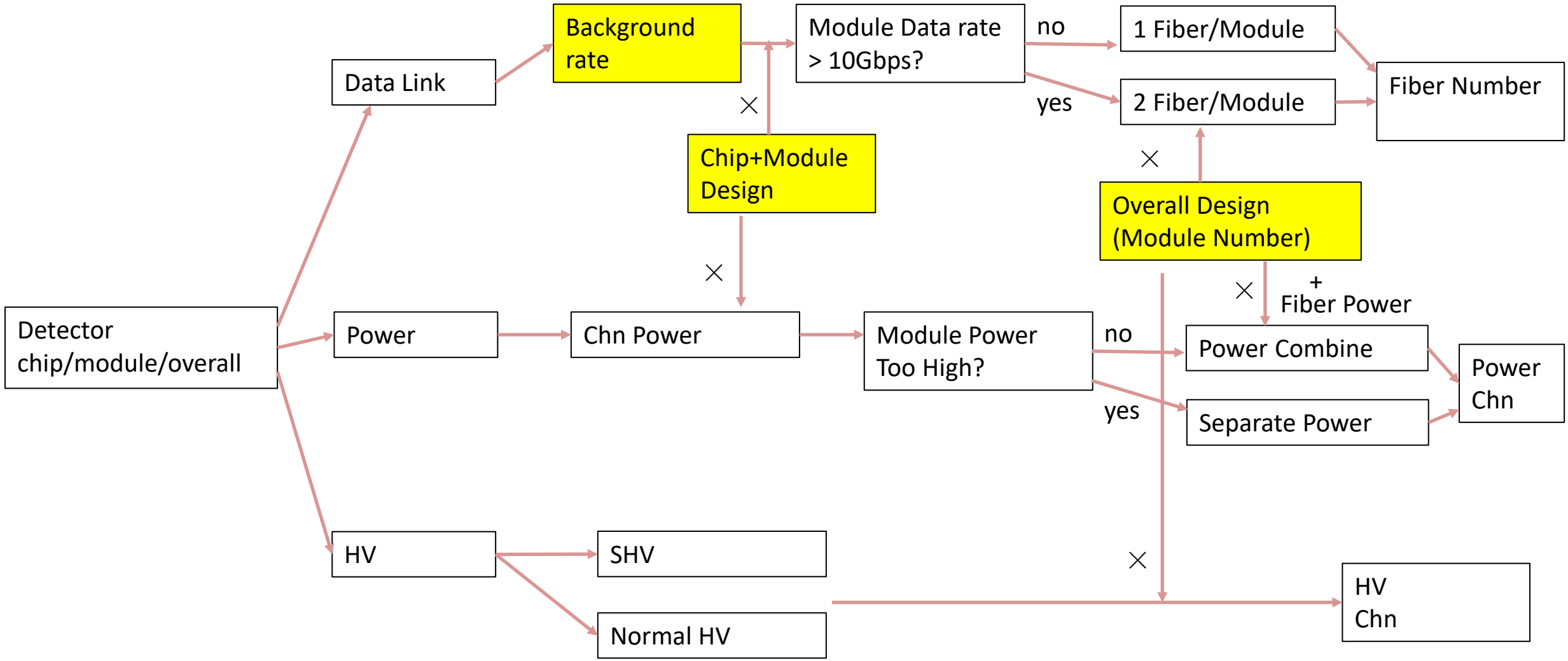
- Minimum crates from current MDI
  - 107 data crates, 227 power crates, 78 Det-HV crates, 20 Trigger crates
- Minimum racks from current MDI
  - 37 data racks, 24 power racks, 23 Det-HV racks, 10 trigger racks (94 in total)
  - More 2 racks for AC-DC power for all the above racks
  - 96 racks in total
- Racks Size: 0.5m × 0.5m
- Side clearance 1.5m for heat, face clearance 2m for cabling & heat
  - Very rough estimation: 20% more power will be consumed due to the crate efficiency
- Total room: 500m^2×2floor = 25m × 20m × 2floor
  - 10 × 10 × 2=200 racks capacity
  - Necessary redundancy for future upgrade



See Quan Ji's talk on Mechanics



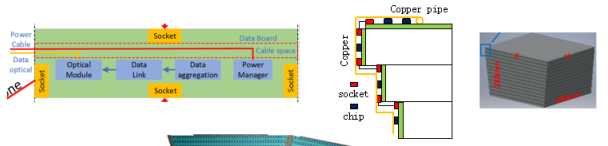
Consideration according to the detector design

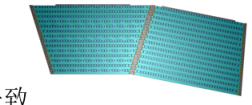


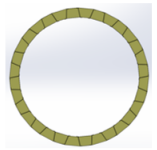
An example of sub-detector consideration (ECAL)

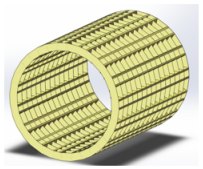
ECAL电缆估算

- ECAL桶部，正反梯形排布
  - 模块数量：Phi：32，Z：15，共480个模块
- 每个模块：
  - 1层到28层，奇数层每层36根，偶数层晶体数目不一致
  - 正梯形晶体数量1000，反梯形晶体数量992
- 电缆估算：1根/模块
  - AWG15（线径1.45mm，电流：6.5A/7.4A）
  - AWG18（线径1.08mm，电流：3.2A/3.7A）
  - 模块功耗估计：1000*2*20mW = 40W
- 光纤估算：1根/模块
  - 模块数据量估算：待定
- 桶部电缆总计
  - 类型：高压，低压（正负？），光纤
  - 电缆双向走向，每端240根（平均方案）
  - 电缆双向走向，一端224根，一端256根
- 未确定电缆：刻度方案

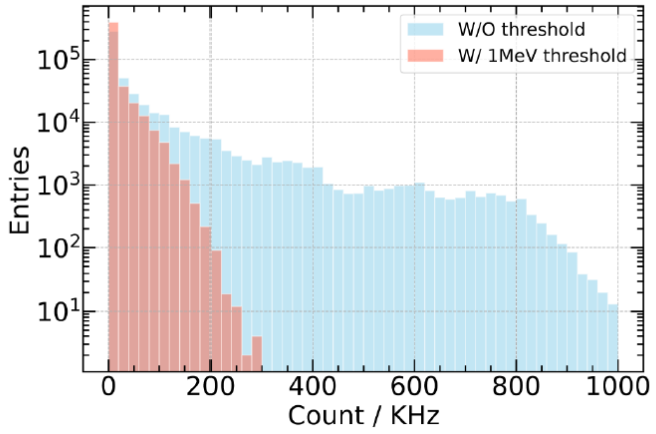








层数	反梯形	正梯形
2	27	39
4	29	37
6	29	37
8	31	37
10	31	37
12	33	37
14	35	35
16	35	35
18	37	35
20	37	35
22	39	33
24	41	33
26	41	33
28	43	33



- The overall detector design: ~480 Module (Dual-trapezium scheme), ~1000 bar/module
- Current bkgrd estimation: avg. event rate 100kHz / crystal bar w/ threshold; Data width 48bit/event (current ASIC scheme)
- @Dual readout each crystal bar, total data rate: 1000*100kHz*48bit*2ends=9.6Gbps, not possible for 1 fiber for each module, at least 2 fibers for each module
  - For max. bkgrd rate@300kHz@Higgs, also needs enough room
  - For Z pole, bkgrd will be much higher, also needs extra room

An example of sub-detector consideration (ECAL)

- Data Link:
  - Fibers: 480*2=960, -> 60 BEE Brds, 6 crates
- Power:
  - ASIC: 15mW/ch, each module 1000*2*15mW=30W
    - Within the capability of DC-DC power module
  - Data Link + Optical Power: 1W each
  - Total Power: 31W/0.85*480=17.5kW
    - Efficiency of the DC-DC: 85%
  - Power chn 100W/chn, each module per power cable: 480 power chn -> power crates 10
- HV:
  - Sch 1: one HV chn for each module, (limitedly) compensated for each SiPM in ASICs
  - HV channels = module number = 480， -> 2 HV crates

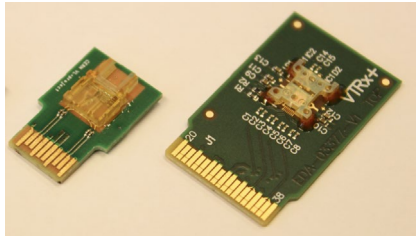
  - Alt sch2：HV chn for each SiPM? Too many channels & too large control data volume (×)
  - Alt sch3：HV chn for sub-region of a module, to compensate the temperature gradient
    - Maybe much optimized than sch1，but rely on the detector simulation

Note for the calculation

- Avg. & Max background rate both are important
  - Max bkgrd rate to calculate the room for the data rate
  - Avg bkgrd rate to calculate the total data rate for the electronics –TDAQ interface
- Detailed detector design, including the module vs. chip, is necessary for the electronics cabling, powering and HV scheme
  - Chip on module to evaluate electronics readout scheme (data link, power, aggregation)
  - Overall detector design to evaluate the cabling, HV and crate channels
- According to the current electronics design, most detector module following the “1 fiber + 1 Power” manner
  - Most module data rate at the level of Gbps, a fiber channels @10Gbps level is proper
  - Although the room for a power channel at the module level is large, current scheme not consider power channel merge
    - Otherwise needs extra power aggregation board on detector, means extra room and increasing difficulty for Mechanics
    - Several detector with enough space (esp. endcaps) with very low power, power channel merge can still be considered

Main parameters for the room calculation – Data Crates

- Optical Link
  - By using MTX interface for fibers, multiple fiber channels can be integrated in small unit
    - Can be 1Rx + 4Tx as a normal design
  - Each Tx channel at 10Gbps rate, with 8b10b protocol, and the max valid data rate to be 8Gbps
    - Major constraint for the detector module
    - If module data rate too high (>8Gbps valid data), multiple Tx fiber channels should be used, while the size of the optical module unchanged
- Crates for data
  - The common BEE Board considered with 16 optical channels, each @10Gbps/Link
  - BEE Board to be designed following the µTCA standard
    - µTCA crate height 9U, total room for 14 cards
    - 2 Ctrl cards for each crate, 1 TTC card (clocking), 1 reserved card
    - 10 valid slots for BEE boards in each data crate
- Racks for data
  - Height of a rack 42U
  - Height for the heat dissipation 2U each
  - Reserve some room for the possible Switch to DAQ
  - Max 3 crates in each Data Rack (= 30 BEE Boards = 480 optical channel)



VTRx+
4Tx + 1Rx
Array Optical Module

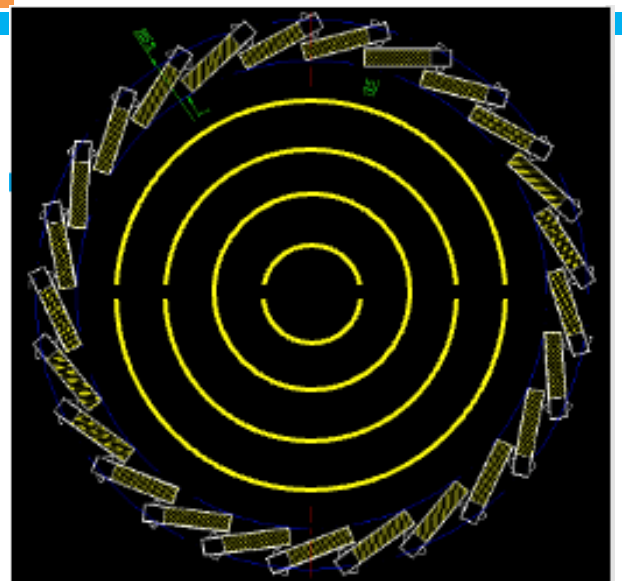
Main parameters for the room calculation – Power Crates

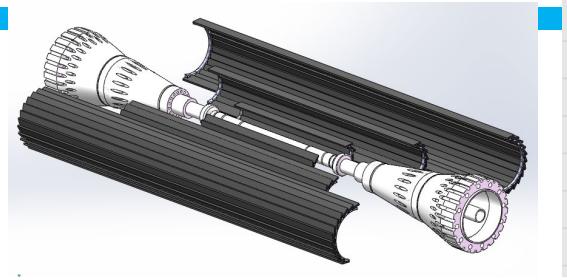
- MV(110V DC to 48V DC) Power Crate & Racks:
  - In the electronics room, near the Data Racks
  - A crate with a height 3U
    - Type1： 48 channels, with the capability of 100W output for each channel
    - Type2: 96 channels, with the capability of 40W output for each channel
  - Concerning the room for heat dissipation, a 42U Power Rack for 10 Power Crates is proper
- Pwr-HV (380V AC to 110 DC) Power Crate & Racks:
  - Power for the MV Power Racks, may be on the ground or far from radiation
  - A crate with a height 6U & total power of 60kW~70kW for a total 10 channels
  - A rack for 5 power crates (6U + 2U cooling)

Main parameters for the room calculation – Det-HV Crates

- Detector HV crates & racks
  - Usually the power of the detector HV source is low, channel density is the major constraint
  - (Ref. from the Det-HV crates provided for ATLAS-HGTD) a crate with a height 8U with 14×16=224 channels, independent tuning for each channel
  - 2U height for heat dissipation for each crate
  - A 42U Det-HV Rack can hold 4 Det-HV Crates
    - If SHV is needed (as for TPC), SHV-connector is larger, height of the crate -> 10~12U, and a Det-SHV Rack will be for 3 Det-SHV crates

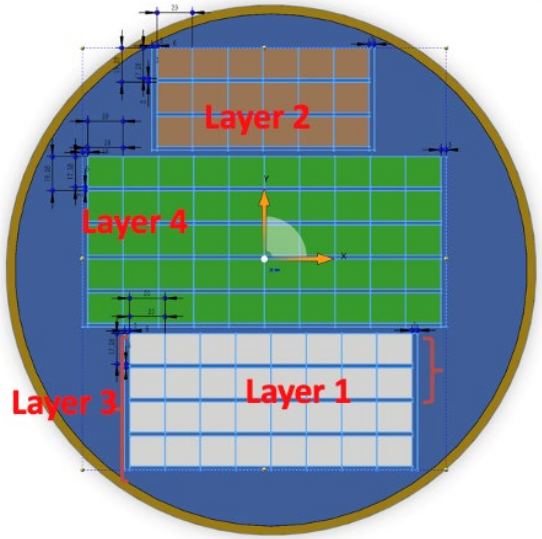
VTX-Data





	A	B	C	D	E	F
1	Layer	Hit density (Hits/cm2/BX)	BXRate (Hz)	Hit density (kHits/cm2/s)	Safe factor	Cluster size
2	VTX-1 (Higgs)	0.65	1.34E+06	870	1.5	3
3	VTX-2 (Higgs)	0.43		580	1.5	
4	VTX-3 (Higgs)	0.09		116	1.5	
5	VTX-4 (Higgs)	0.08		110	1.5	
6	VTX-5 (Higgs)	0.05		70	1.5	
7	VTX-6(Higgs)	0.05		68	1.5	

- VTX scheme: Inner 4 layers stitching, with 1 typical double-sided ladder (layer 5&6)
- Bkgrd rate @50MW @Higgs with safety factor 1.5
- Assume RSU@stitching = ladder chip = 1024*512 matrix, then data rate for the innermost layer for a “chip” is 2Gbps, other layers according the bkgrd ratio
- Inner 2 layers needs 2 fiber chns for each row, due to the high data rate
  - possible to merge into less optical MTX interfaces
- In total 88 fibers = 6 BEE Brd = 1 Data Crate



From Zhijun

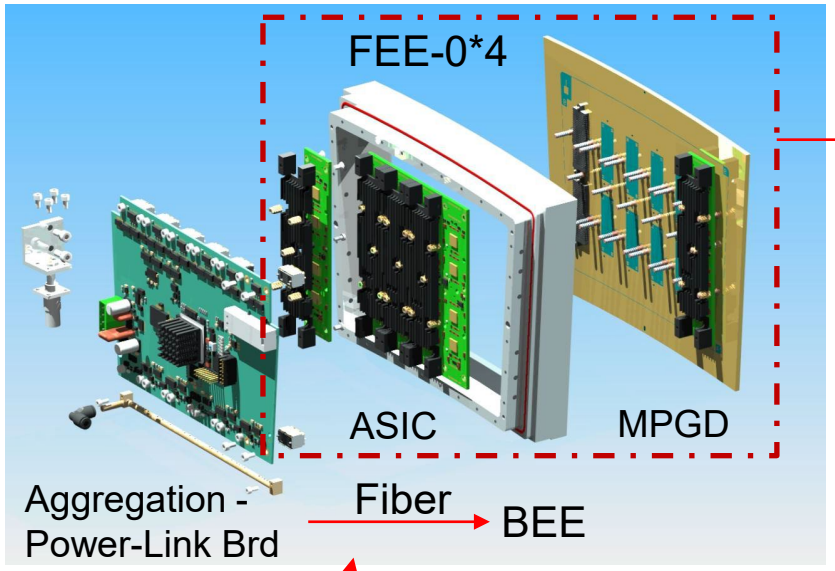
Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8（2 fiber chns）
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12（2 fiber chns）
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25

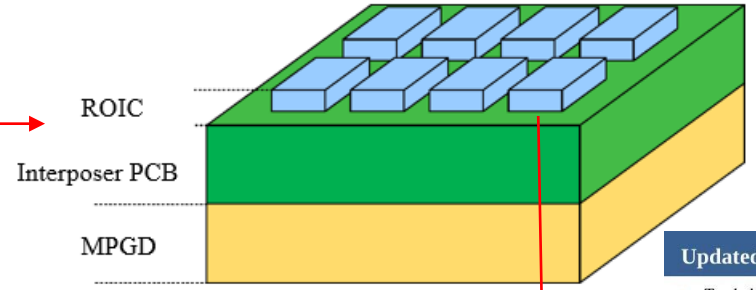
VTX-Power

Layer	Comment	Power/chip	Chips/Row	Power /row	Rows	Chip Power of Layers	Total Power/Layer (Chip+Link) *1.18
1	Stitching	200mW	8	1.6W	2*2=4	6.4W	(6.4+4) *1.18=12.2
2	Stitching	200mW	12	2.4W	3*2=6	14.4W	(14.4+6) *1.18=24
3	Stitching	200mW	16	3.2W	4*2=8	25.6W	(25.6+8) *1.18=39.5
4	Stitching	200mW	20	4W	5*2=10	40W	(40+10) *1.18=58.8
5	Ladder-side0	200mW	29	5.8W	25	145W	(145+25) *1.18=200
6	Ladder-side1	200mW	29	5.8W	25	145W	(145+25) *1.18=200

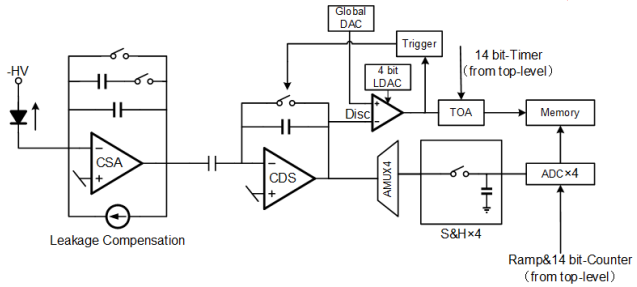
- For simplicity, assume the power of Unit(RSU/Chip) is the same 200mW(40mW/cm2 * 2.6cm*1.6cm)
  - Main contribution of power: analog static power + data link, not varying with bkgrd rate
- Extra cost by using optical: fixed 1W each set
  - 0.75W for Data Interface & 0.25W for 1 Rx+4Tx VTRx
- Efficiency of PAL DC-DC is 85% = extra efficiency cost of DC-DC 18% (1÷85%=118%)
- Total power: 449.8W
  - 16 power channels each layer for 1~4, each chn for a semi-; 2 chn for each ladder in 5/6 layer, 50 chn in all
  - Power will be provided from both ends for long barrel
  - 66 power channels = 2 power crate
    - Very likely to be merged due to the limited room for VTX

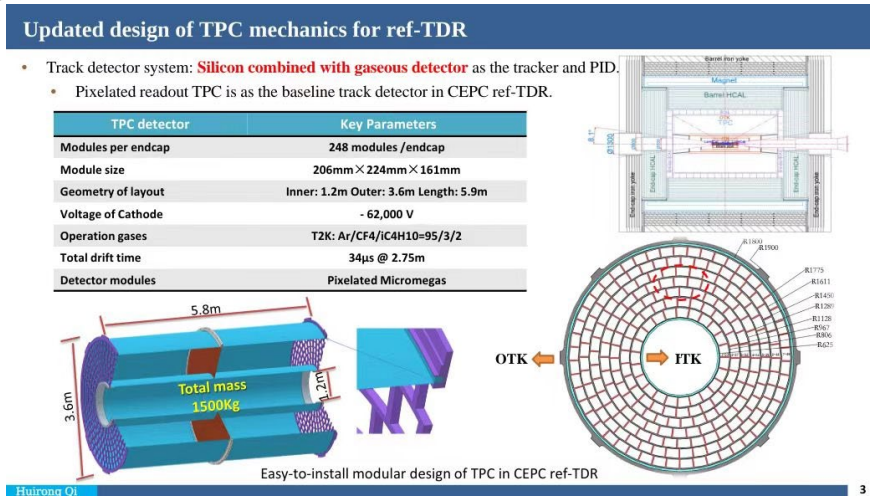
Preliminary readout scheme of Pixel TPC



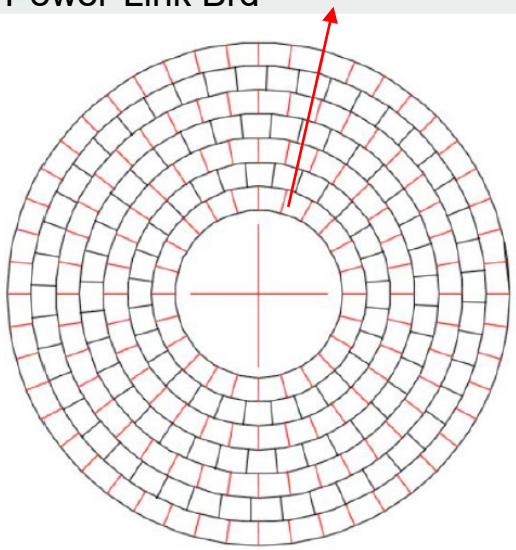


An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





From Huirong



~248 Module/Endplate

128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0

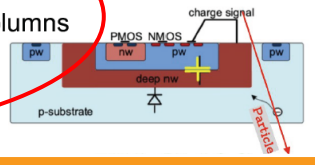
Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn

Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

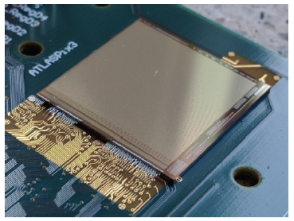
ITK——Power (Barrel)

Technology Survey and our Choice for ITK: Option 1

- CMOS sensor technology:
  - Cost-effective due to widespread use in the semiconductor industry
  - Combine the active detection layer and the readout electronics into a single device
- HVCMOS pixels:
  - Large depletion depth (full depletion), large signal
  - Radiation hard
  - Relatively large capacitance, leading to increased noise and power consumption
- New HVMOS (COFFEE) pixels R&D for CEPC:
  - Utilizes 55 nm process instead of the 180 nm used in ATLASPix3
    More functionality and less power consumption
  - Wafer resistivity: 1k-2k Ω·cm
  - Pixel size: 34 × 150 μm²
  - Array size: 512 rows × 128 columns
  - Power consumption: ~200 mW/cm²



- ATLASPix3
  - TSI 180nm HVCMOS on 200 Ωcm substrate
  - Pixel size 50 × 150 μm²
  - 372 rows × 132 columns
  - 20.2 × 21 mm² reticle size
  - Each pixel has 7-bit TOT + 10-bit timestamp
  - Continuous / triggered readout with 8b10b / 64b66b coding
  - Power consumption ~160 mW/cm².



4

ITKB	Modules/layer	Layer power (W)	Data Link Power (W)	Total Power(chip+data) /85%
1	280	3.14k	280	4.02kW
2	580	6.50k	580	8.32kW
3	1344	15.1k	1344	19.29kW

- Estimated chip power 200mW/cm², 14 chips per module, Module power 11.2W
- Extra power: Data Link 1W per module
- 1 Power channel for each module for reliability & installation simplicity
- Power channels: 280 + 580 +1344=2204, -> Power Crates 3+12+14=29, each layer independent
- HV range 50~200V (normal HV), independent tuning for each module
  - Det-HV channels also 2204, -> Det-HV Crates 10

ITK——Data Link (Endcap)

Hit Rate Conclusion

	Z [mm]	R_in [mm]	R_out [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKE1	500.5	75	240	3.9	23
ITKE2	715	101.9	350	16	38
ITKE3	1001	142.6	600	8.9	75
ITKE4	1500	213.7	600	2.4	6.3
OTKE	2903	406	1810	0.3	3.5

	R [mm]	Half_Z [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKB1	240	500.5	1	4.6
ITKB2	350	715	2.1	41
ITKB3	600	1001	2.1	27
OTKB	1800	2000	0.7	0.9

Endcap	1 (per Sector)	2	3	4	Total
Ladder Type	6	8	15	12	18
Ladder Number	7	10	18	15	1600
Chip Number	48	98	260	236	20544
Active Area (mm^2)	20181.03	42796.32	116080.28	106081.77	9.12e6
Module Area (mm^2)	23184	47334	125580	113988	9.92e6
Power Consumption (W)	46.368	94.668	251.16	227.98	1.98e4
Avg. Hit Rate (Hz/mm^2)	3.9e2	1.6e3	8.9e2	2.4e2	-
Data Rate (Hz)	2.89e8	2.42e9	3.58e9	8.75e8	2.29e11

ITKE	Ladder Max chips	Avg bkgrd rate (Hz/cm^2)	Max bkgrd rate (Hz/cm^2)	Avg Module Data rate (Mbps)	Max Module Data rate (Mbps)	Modules/Ladders(Fibers)
1	9	39k	230k	47.2	278.4	7*8*2layer*2Endcap =224
2	13	160k	380k	279.7	664.3	10*32=320
3	22	89k	750k	263.3	**2218.9**	19*32=608
4	22	24k	63k	71.0	186.4	17*32=544

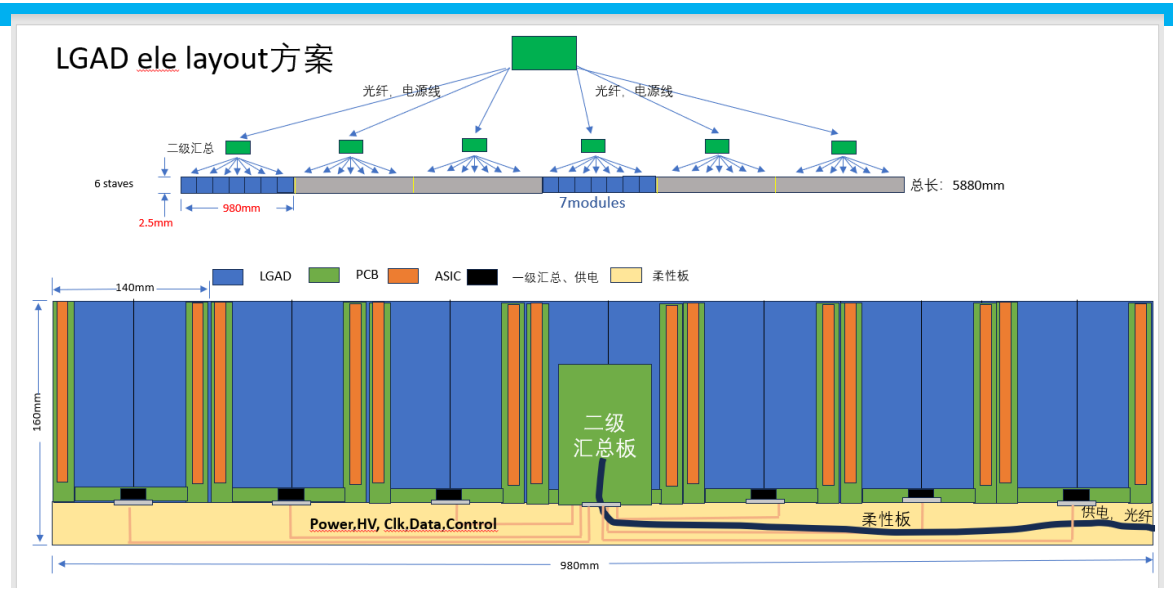
- Max module data rate 2.2Gbps, enough room left by using 1 fiber for each ladder
- Ladders in total：224+320+608+544=1696，=106 BEE，=12 Data Crates (symmetry from two side)

OTK-Data Link

Hit Rate Conclusion

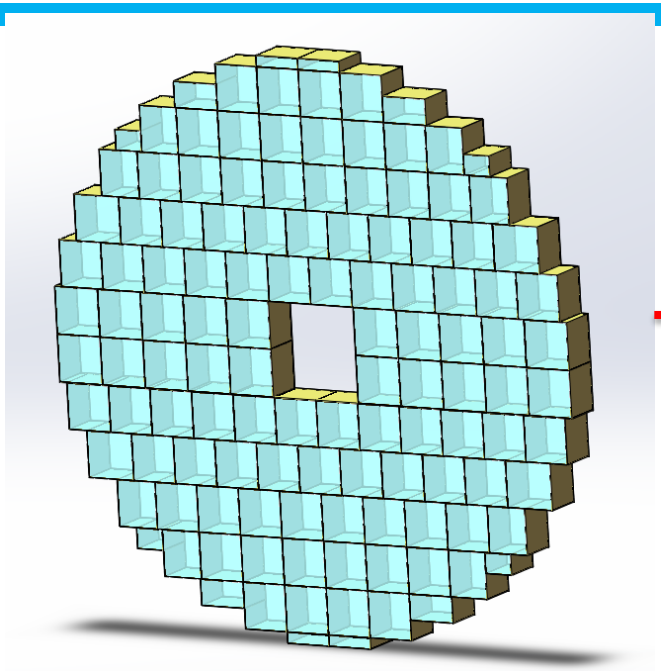
	Z [mm]	R_in [mm]	R_out [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKE1	500.5	75	240	3.9	23
ITKE2	715	101.9	350	16	38
ITKE3	1001	142.6	600	8.9	75
ITKE4	1500	213.7	600	2.4	6.3
OTKE	2903	406	1810	0.3	3.5

	R [mm]	Half_Z [mm]	Average hit rate [10^4 Hz/cm^2]	Max hit rate [10^4 Hz/cm^2]
ITKB1	240	500.5	1	4.6
ITKB2	350	715	2.1	41
ITKB3	600	1001	2.1	27
OTKB	1800	2000	0.7	0.9

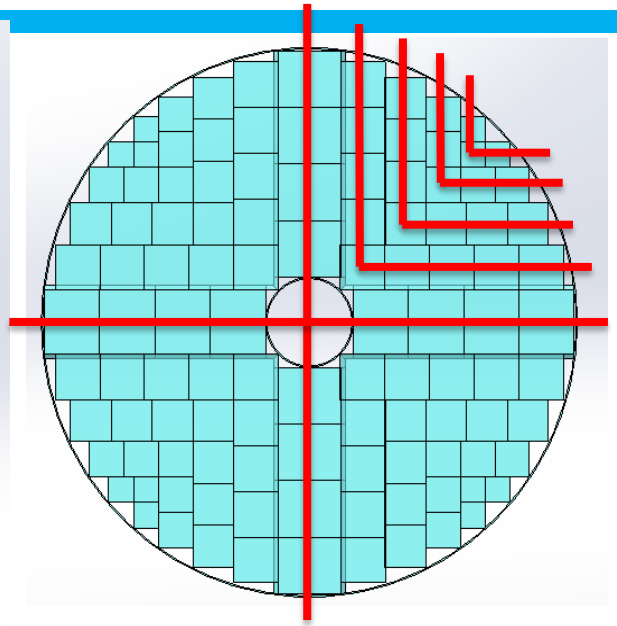


- Barrel:
  - Data link proposed to locate at the 2nd level aggregation board, for 7 modules (1 ladder), each module 22 ASICs
  - Avg module rate 7kHz*14cm*14cm*48bit=65.9Mbps, Max 9kHz→84.7Mbps
  - For the optical data rate of 7 modules (1 ladder), avg/max to be 461.3Mbps/1355.2Mbps, with large room for the data link
  - A full 6m Stave with 6 Ladders (6 fibers), barrel in total 90 ladders, =540 fibers = 34 BEE = 4 Data Crates
- Endcap:
  - 48 Pedals for 2 endcaps, 10 rings each Pedal with 15 sectors (Inner 5 rings 1 sector, Outer 5 rings 2 sectors)
  - Total area 19.4m^2, =4041.7cm^2 for each Pedal, avg. Pedal data rate= 3kHz*4041.7*48bit=582Mbps, Max 35kHz→6.79Gbps
    - Consideration 1 fiber for each sector, even concerning the higher data rate for inner sectors, enough room left for the fiber
  - 48 Pedals with 720 sectors in total, =720 fibers = 45 BEE = 6 Data Crates (each endcap independent)

ECAL – endcap



Original design



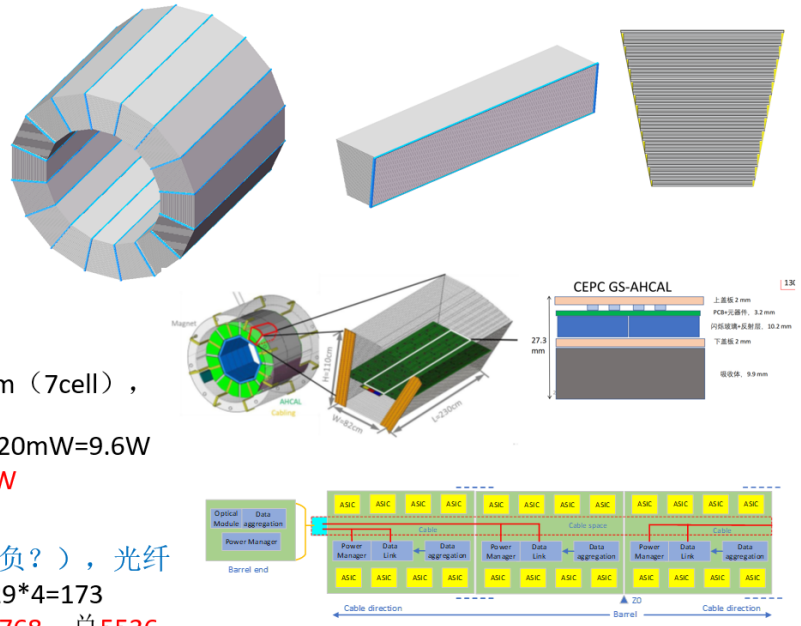
In optimization

- Waiting for the final design of ECAL endcap
- According to the current design, module number 122~96, calculated by 130 modules
- Expect higher bkgrd rate than barrel, keep the scheme of 2 fibers per module
- Fibers:
  - 130module*2endcap*2 fiber=520
  - 34 BEE = 4 Data Crates (from 2 sides)
- Power：
  - Total power: 31W/0.85*260=9.48kW
  - 260 Power channels = 4 power crates

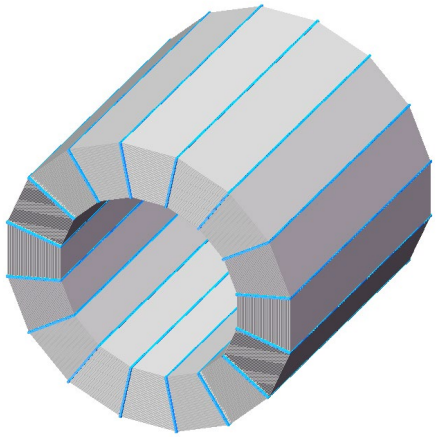
HCAL-Data Link(barrel)

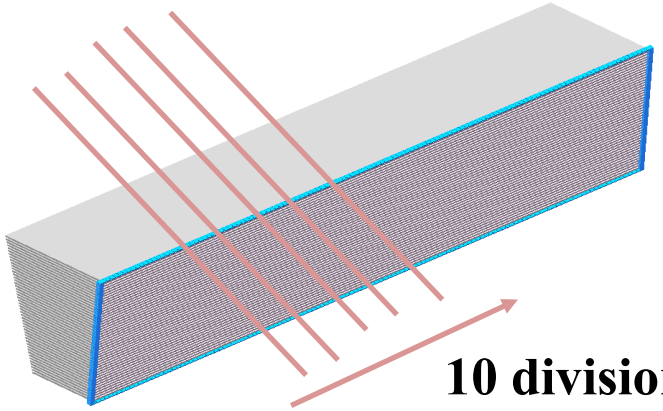
HCAL电缆估算

- HCAL桶部排布
  - 总通道数：338万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 电子学板尺寸
  - Z向：60cm（15cell）
  - Phi向：24cm（6cell），28cm（7cell），32cm（8cell）
  - FEE单板最大功耗：15*8*4*20mW=9.6W
  - 汇总板最大功耗：9.6*5=48W
- 桶部电缆数量
  - 电缆类型：高压，低压（正负？），光纤
  - 1/16 分区电缆数量：19*3+29*4=173
  - 总电缆数量：一端173*16=2768，总5536
  - AWG12（线径2.05mm，电流：13.1A/14.9A）

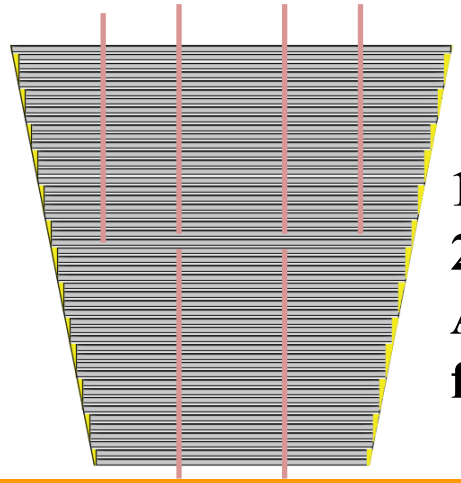


- Currently, HCAL is not finalized, especially for the module design, e.g. cell size and channel number
- Data have to be aggregated at the end of barrel for each layer, also the DC-DC
- By rough estimation, the bkgrd will be low（5kHz/GS），the aggregated data rate for each layer board should not exceed 8Gbps (10Gbps for the fiber)
  - Then 1 fiber for each aggregation board is reasonable
- Fibers：
  - Aggr. board number every 1/16 sector：19*3+29*4=173
  - 1 fiber per aggregation board: 173*16*2=5536 fibers
  - =346 BEE = 36 Data Crates





10 divisions

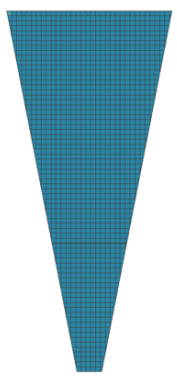


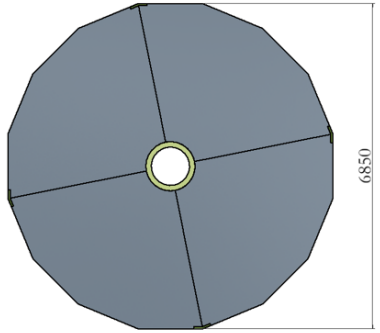
1~19layer 3PCBs width
20~48layer 4PCBs width
Aggr Brd for 5 PCBs along z from both ends, with 1 fiber

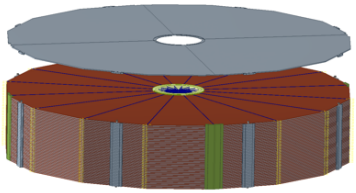
HCAL-Data Link (Endcap)

HCAL电缆估算

- HCAL端盖部排布
  - 总通道数：单端112万，总共224万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 端盖电缆数量
  - 电缆类型：高压，低压（正负？），光纤
  - 每区功耗：1459*20mW=30W
  - 1/16 分区电缆数量：48
  - 总电缆数量：一端48*16=768，总1536
  - AWG12（线径2.05mm，电流：13.1A/14.9A）
- 未确定电缆：刻度方案





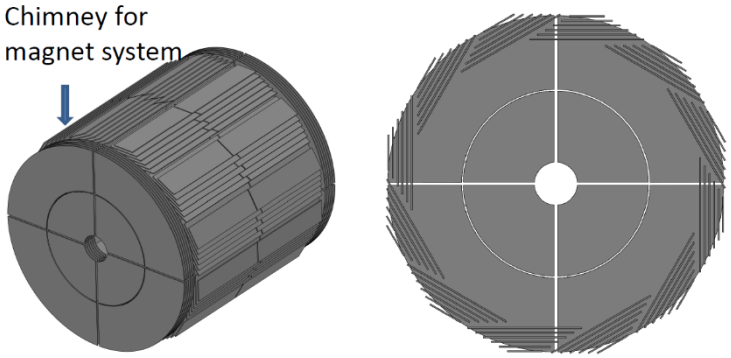


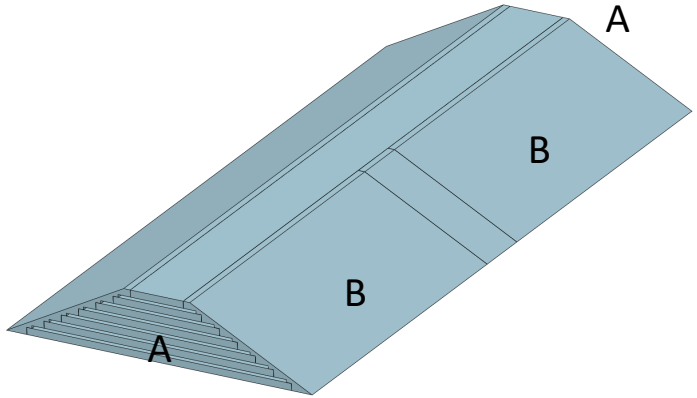
- **Fibers**
  - **1 fiber for each sector at each layer**
  - **48layer*16sector*2endcap*2End-board=3072**
  - **=192BEE = 20 Data Crates**

- Current design for HCAL:
  - 48 layers with 16 sectors
- Needs input of the bkgrd rate, assuming 1 fiber is enough (data rate < 8Gbps) for each sector at each layer
- Rough calculation:
  - each endcap 1.12M channels -> 1458 GS cells for each sector
  - MDI: 50kHz/GS max
  - 1458GS * 50kHz *48bit=3.5Gbps
- Using 2 end-boards for each layer of sector, then each board 1.75Gbps, OK for 1 fiber

Muon - barrel

- Number of channels: (288 modules) $43k$
  - Barrel: 144 modules, 23,976 ch
  - Inner endcaps: 48 modules, 6,912 ch
  - Outer endcaps: 48 modules, 12,288 ch
- Sensitive length: $119\ km$
  - Length for PS bar and WLS fiber
- Sensitive area: $4.8 \times 10^3\ m^2$





- Using side board and end board for data aggregation and power distribution
- Barrel 144 module, each with 2 boards
  - 288 fibers = 18 BEE = 2 data crate
  - Total data rate: <1kHz*23976*48bit=1.15Gbps (each board 4Mbps)
  - Using fiber for universal architecture & clocking precision
  - Total FEE power: 23976*15mW/chn=360W
  - With data link 1W*288=288W, 85% efficiency
  - Total power: 760W
- Endcap 96 module
  - 96 fiber=6 BEE=1data crate
  - Total data rate: <1kHz*19200*48bit=921.6Mbps (each board 10Mbps)
  - Total FEE power: 19200*15mW/chn=288W
  - With data link 1W*96=96W, 85% efficiency
  - Total power: 452W

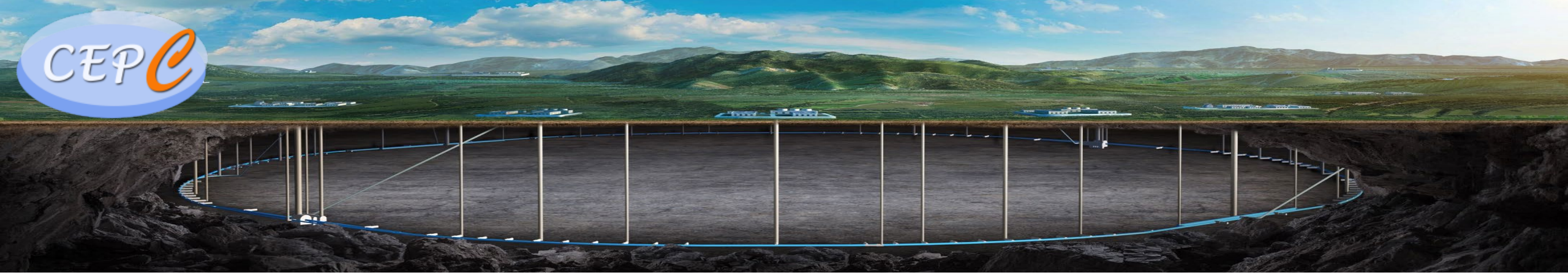
Summary for the Racks

- No safety factor for all the former calculation
- In total
  - 110 Data Crates, 3 crates per rack, = 37 Data Racks
  - 237 (LV) Power Crates, 10 crates per rack, = 24 Power Racks
  - 91 Det-HV Crates, 3/4 crates per rack, = 23 Det-HV Racks
  - 20 Trigger crates = 10 Trigger Racks
- Every LV rack needs an AC-DC power-HV crate, about 134 power-HV crates
  - 5 crates per rack, = 2 Power-HV Racks
- In general, rack backup, room for future upgrade, uncertainty due to the un-finalized detector scheme, esp. the extra space requirements that the trigger algorithm usually asks the rack layout to be corresponded to the detector arrangement, will decrease the density of the rack and crate usage.

In Case…

- In case some high-end commercial chips are not available (due to the high cost or other reasons), if substitute can be found from other possible tunnels?

	FPGA	RAM	DC-DC	LDO	CLK	CLK-PLL	Crate
Substitute exits?	Y	Y	Y	Y	Y	?	Y
Possible tunnels 1~5	1	2	5	5	3	?	2/Cust



BACKUP - Miscellaneous

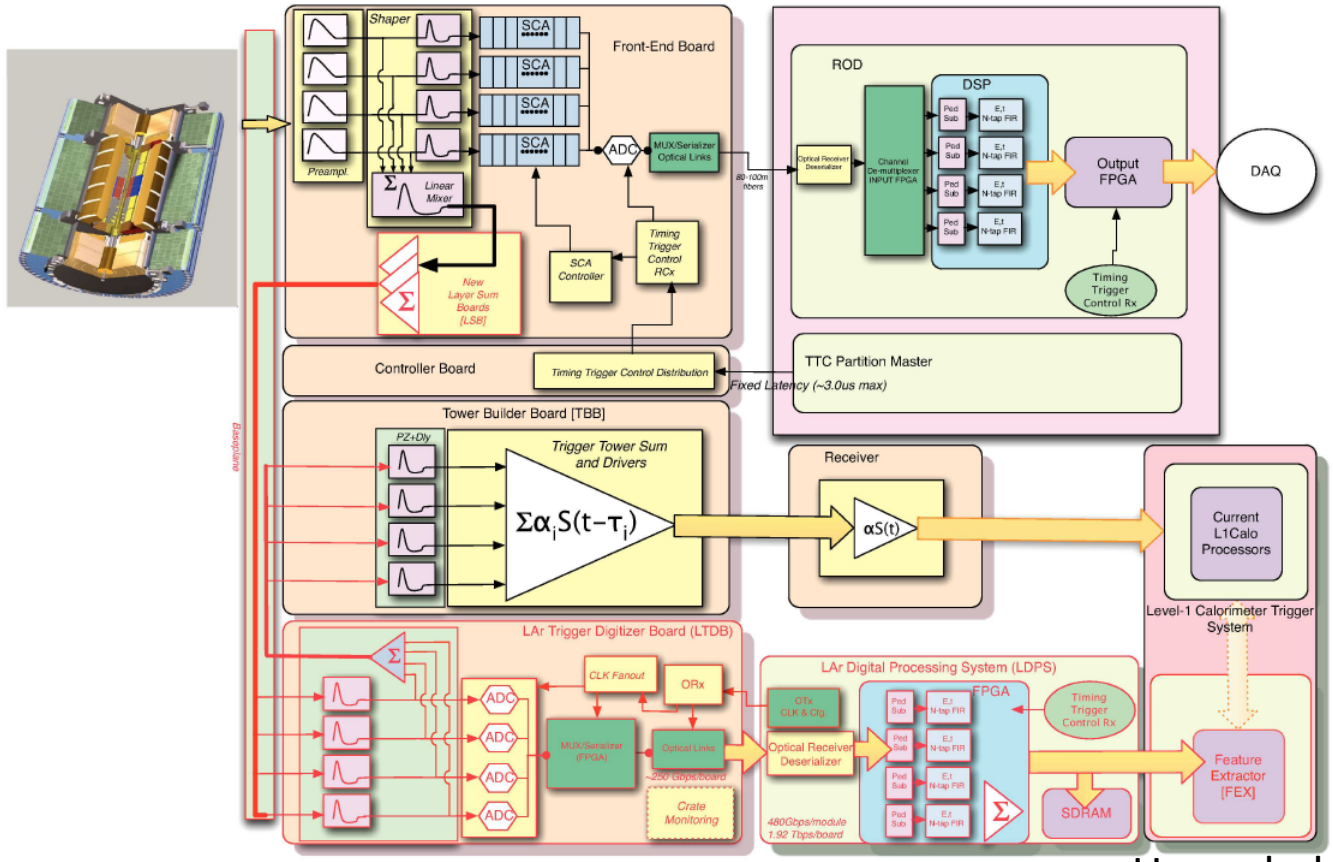
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Working plan on key R&Ds

- Key R&D left to do towards & beyond the Ref-TDR
  - An lpGBT-like chip series (FEDA + FEDI + OAT) should be developed as the common data link platform
    - Transmission protocol, including up(typically FEC12) and down(typically I2C & fast commander), is a key component according the current tech stage
  - GaN based DC-DC module (PAL Series) is also critical for FEE modules in high radiation environment
    - Further radiation tests should be performed, including TID, SEE, and NIEL
  - OTK & SiPM ASIC aiming for a prototype system in 3 years with detectors
  - A prototype based on wireless communication scheme will be demonstrated to show the feasibility (personal power in parallel with the main task)
    - Customized antennas, adapters, and repeaters are being coordinated with the industrial sector in China for a more compact design

Technology survey on global framework

ATL-CAL-PROC-2017-001

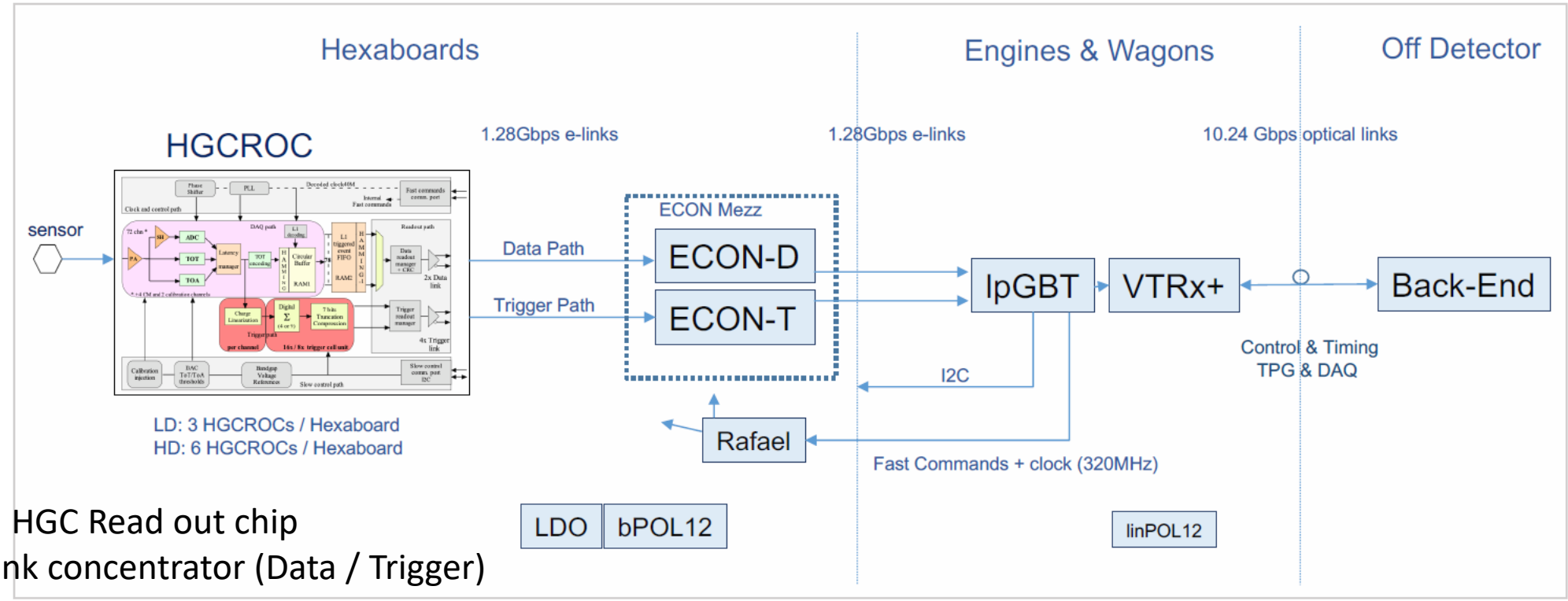


Upgraded LAr readout schemes for Phase-I

- A typical readout framework can be referred to ATLAS detector system(e.g. LAr CAL)
- It can be noted the FEE not only has to generate and send out trigger info.(e.g. SUM), but also store data for trigger latency and accept the trigger decision.

Technology survey on global framework

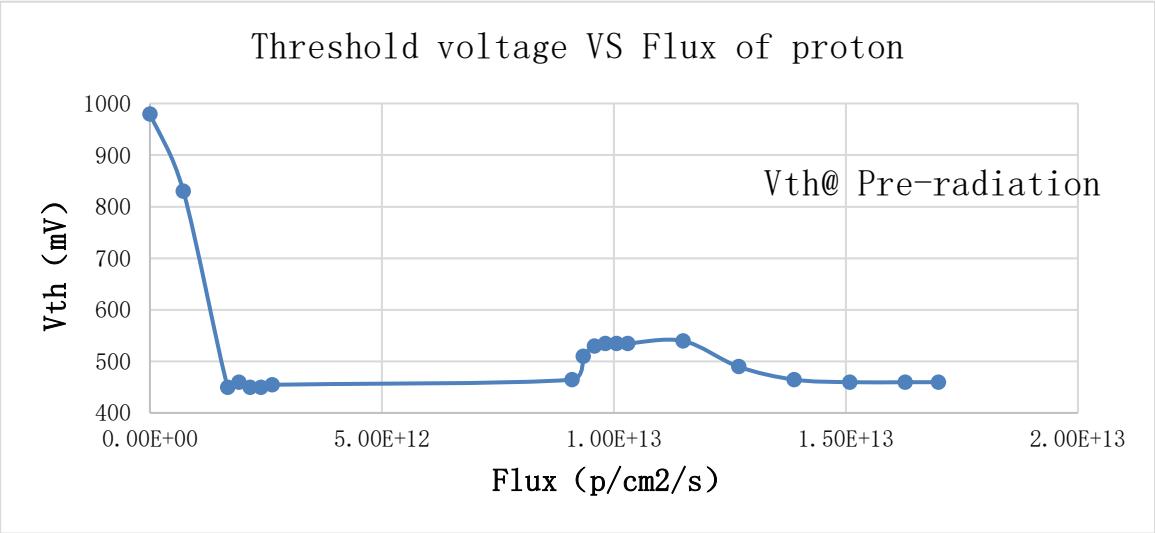
From Paul Aspell, CMS HGCAL An Electronics Perspective



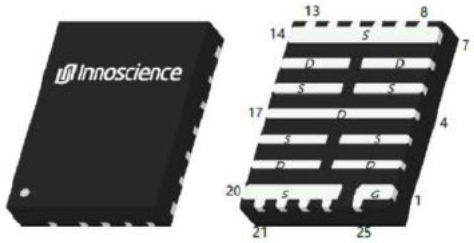
HGCROC: HGC Read out chip
ECON: elink concentrator (Data / Trigger)

- The electronics readout framework can also be inspired by CMS detector system(e.g. HGCAL).
- It can be observed that the data stream is mostly in a single direction to the BEE, and the electronics system architecture is relatively compact.

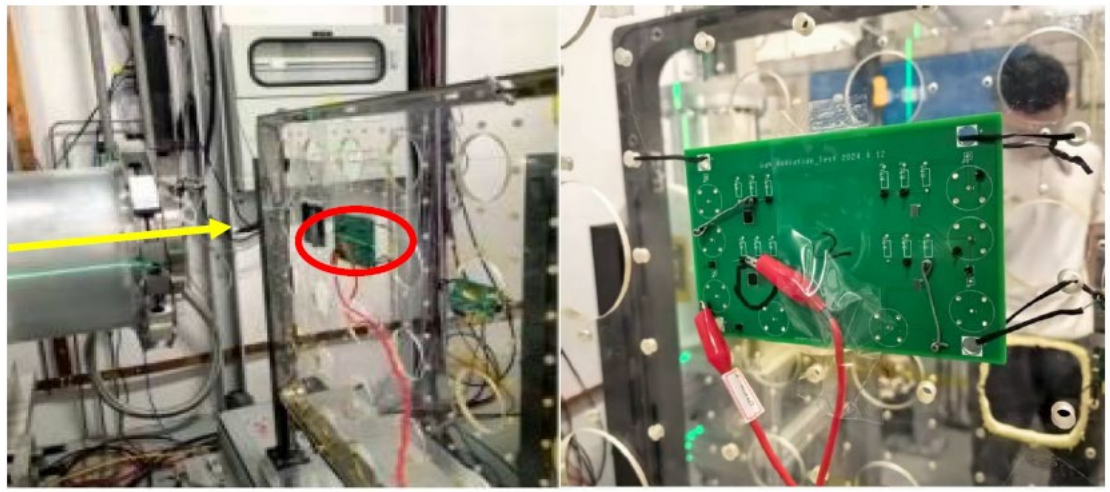
Update on common Power module



- Power requirements summarized according to the current readout schemes of each SubD
- Rad-test of COTS samples initiated, preliminary proved the GaN transistor can survive in the CEPC rad environment
- Recent plan:
  - Key component evaluation



测试仪器：源表、电源、万用表

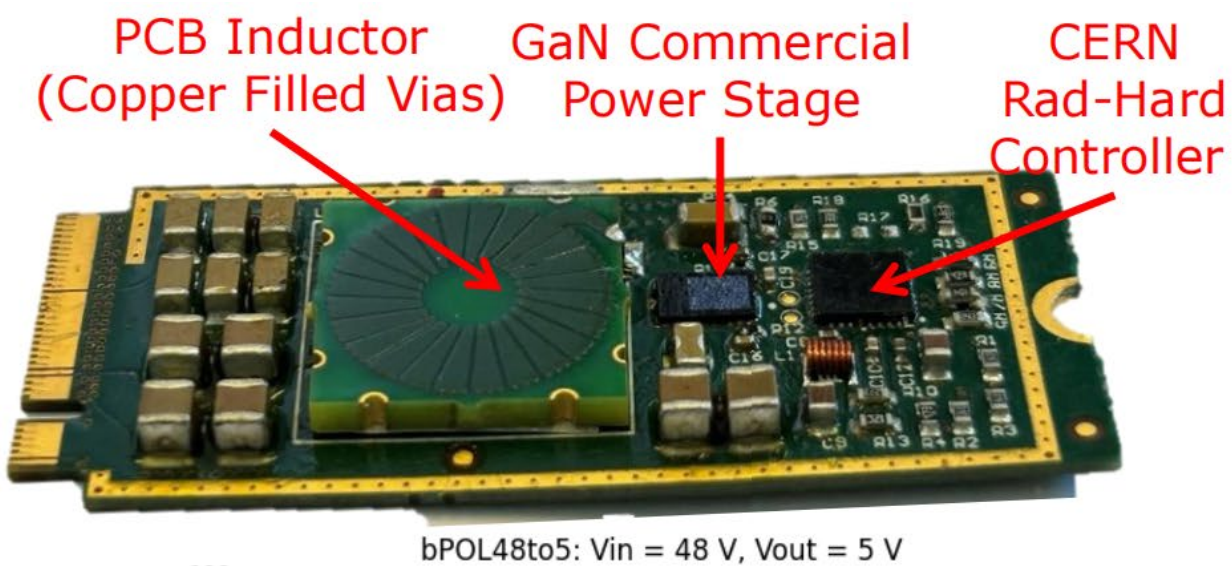


测试PCB固定到样品台上的实物照片(左图中黄色箭头为束流方向)

Using available stock of bPOL48V (~70K dies)

Volume optimized bPOL48 modules:

- bPOL48to12 (EPC2152): 48V to 12V with 6A out
- Dimensions: 24 x 55 x 4 mm



bPOL48to5: Vin = 48 V, Vout = 5 V

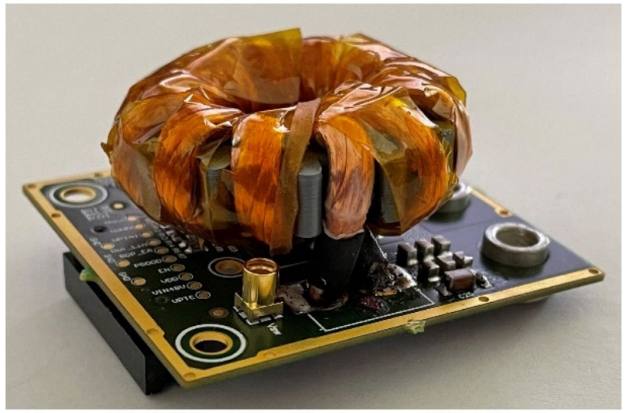


Figure 14: bPOL48V with air-core 220nH inductor.

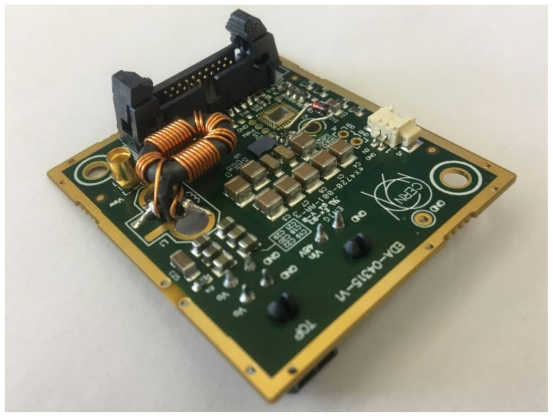
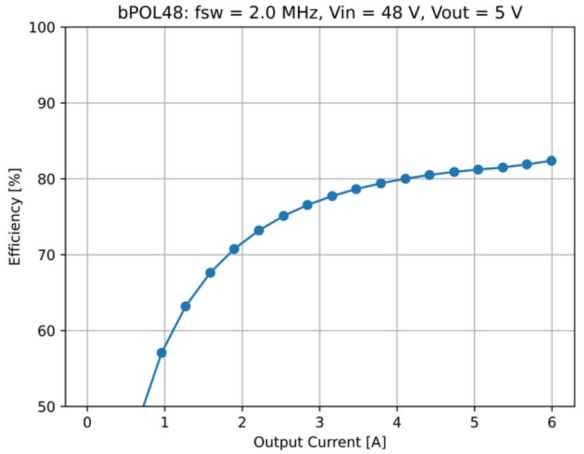
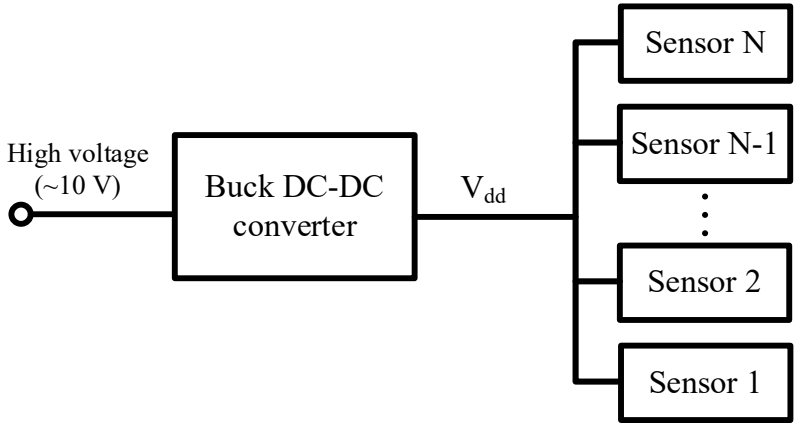


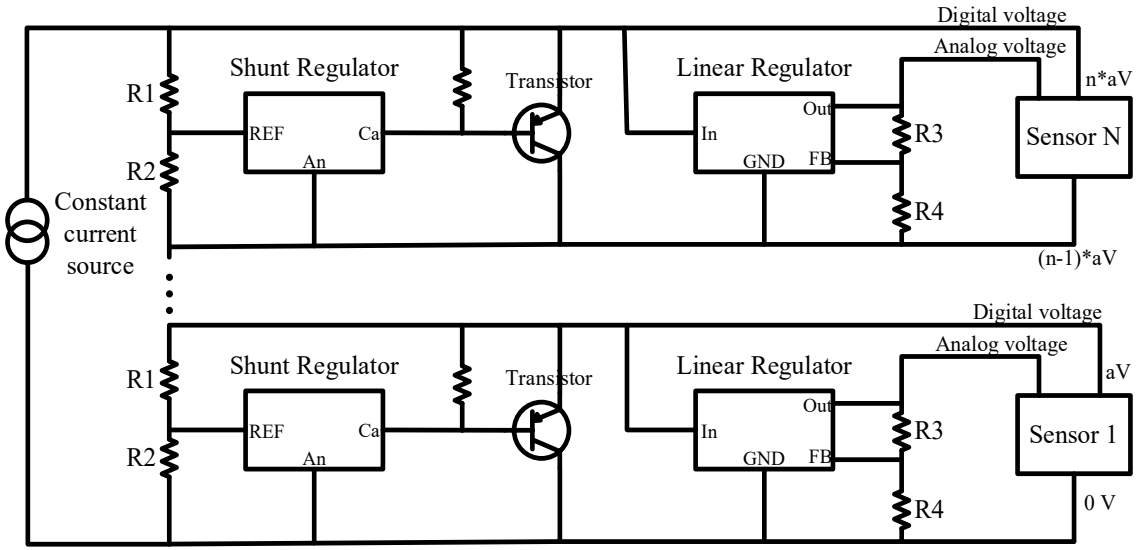
Figure 17. bPOL48V using the FEASTMP inductor.



Technology survey and our choices

- Parallel powering with DC-DC converter VS Serial powering





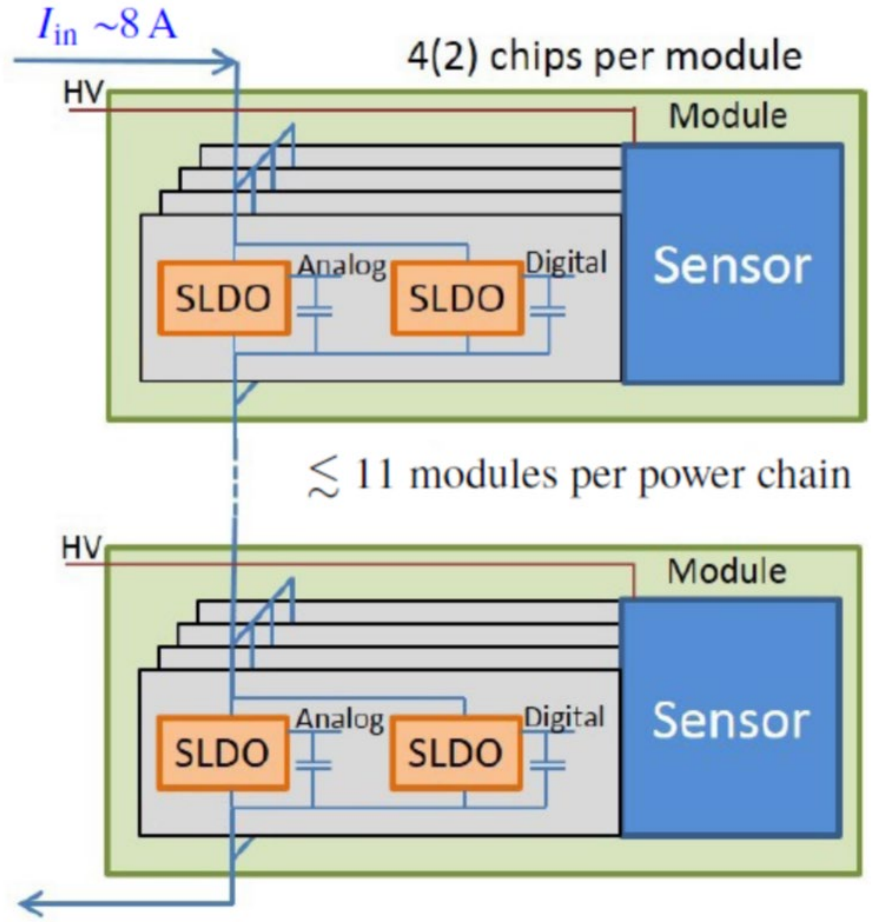
Parallel powering

- ✓ Compatible with the conventional power system
- ✓ Few changes of readout circuit or sensor required
- ✓ High reliability
- ✓ Unecessary on-chip regulator-> less die area
- ✗ Noisy ripple voltage
- ✗ Large-area air-core inductor
- ✗ EMI

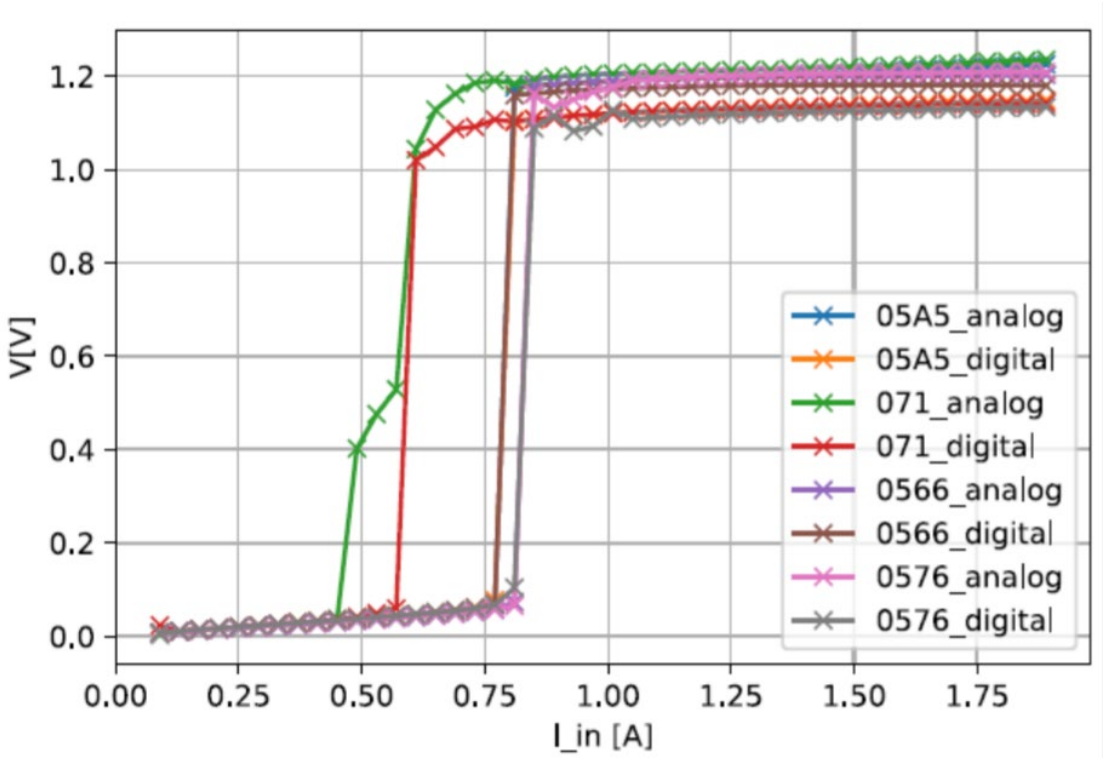
Serial powering

- ✓ Less cable mass
- ✓ Higher power efficiency, more suitable for large current load
- ✓ Low noise
- ✓ Unrequired Magnetic components
- ✗ Many changes with the old power system
- ✗ Lower reliablity
- ✗ Different groud potential -> AC-coupled output, no suitable for stiching chips, very high bias voltage of sensors
- ✗ “Larger” threshold current required to switch on shunt regulator
- ✗ Consistency of shunt regulator and LDO

Backup------Serial powering



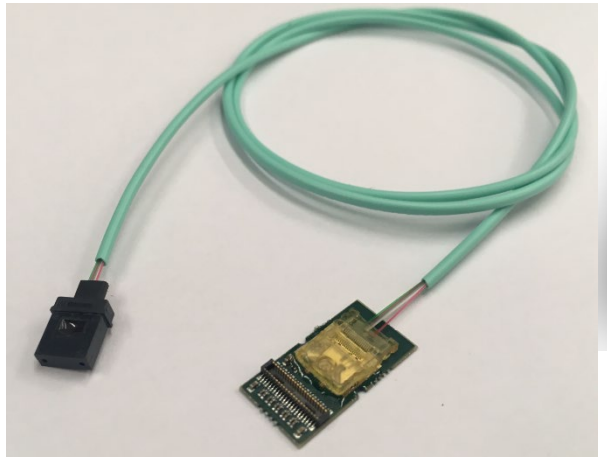
Structure of serial powering for CMS pixel detector

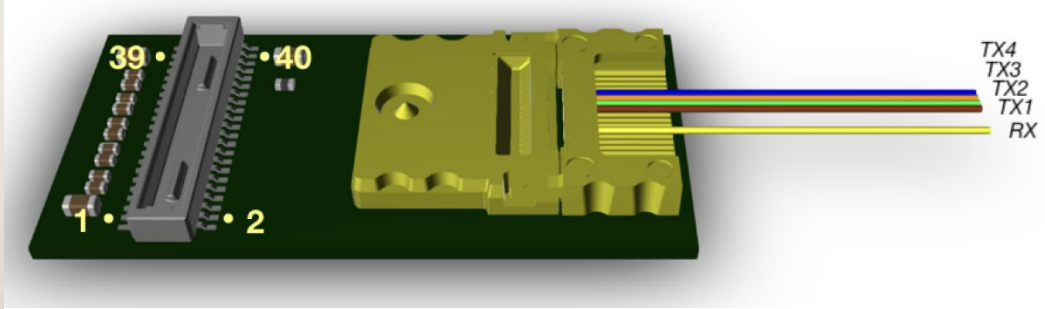


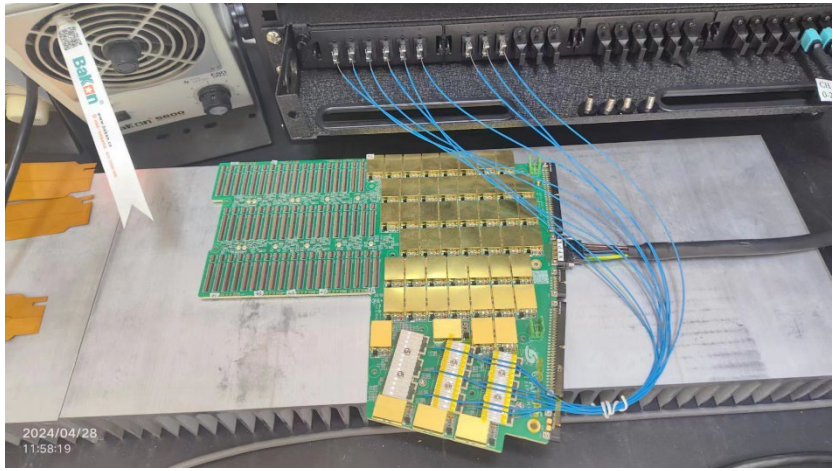
Regulated voltage for four single chips with different switching on current

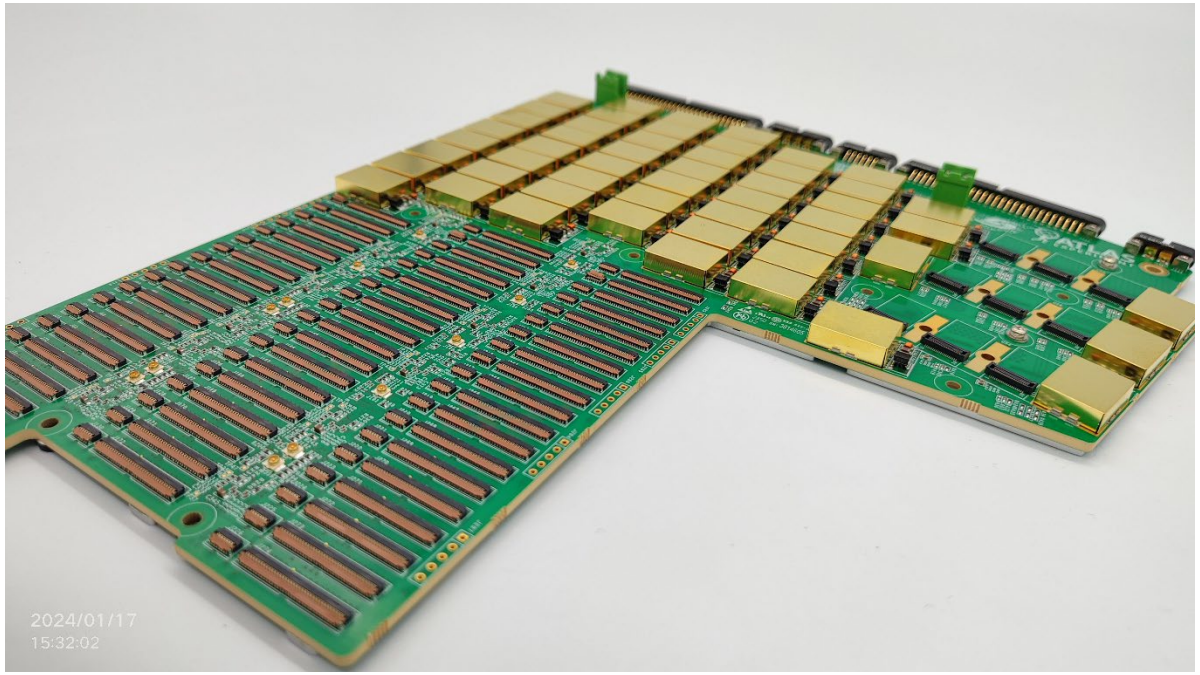
[Vasilije Perovic, Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector, NIMA, Volume 978,2020,164436,]

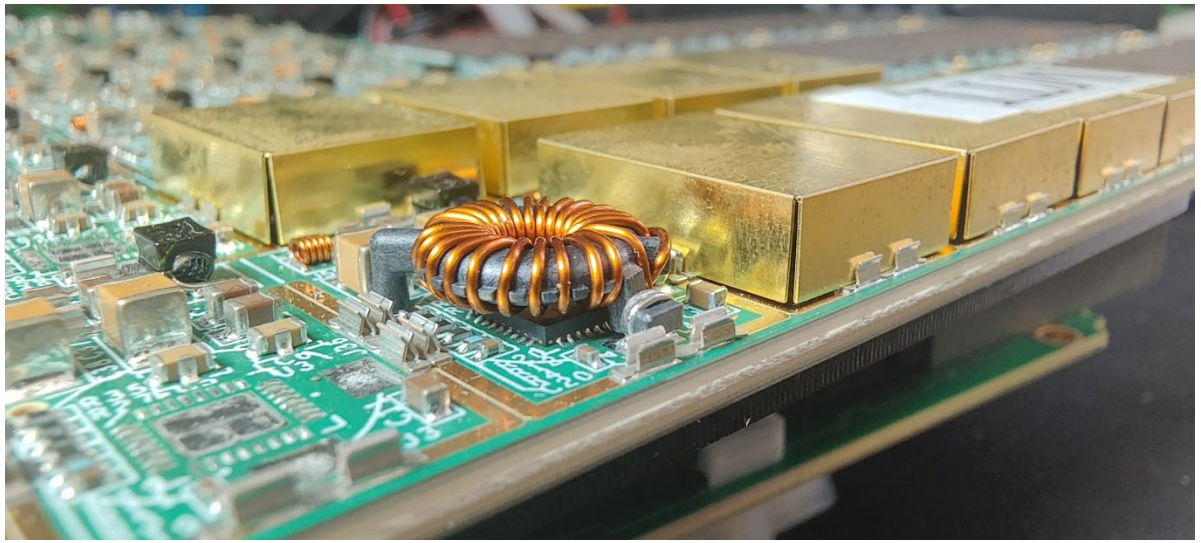
Size of bPol & GBT



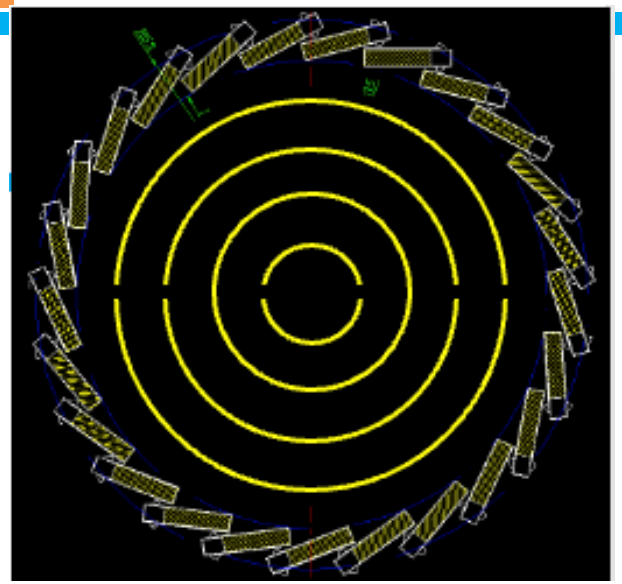


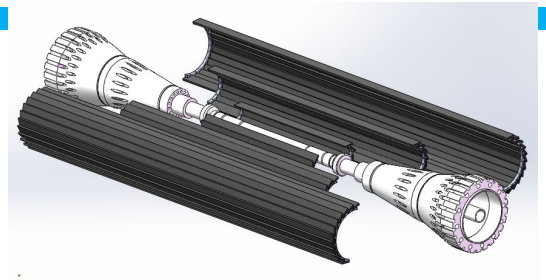


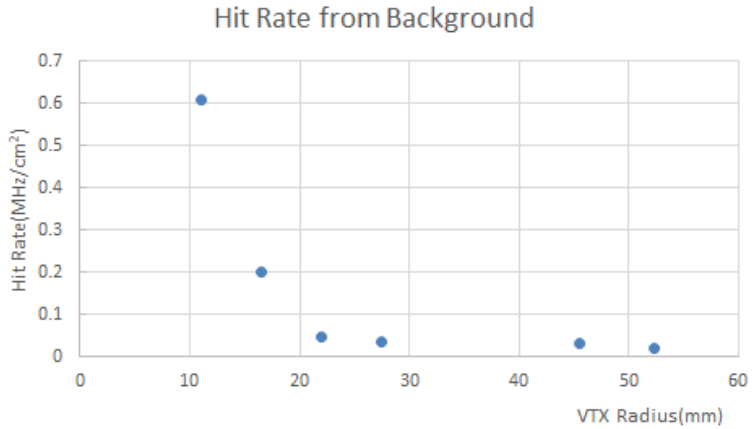




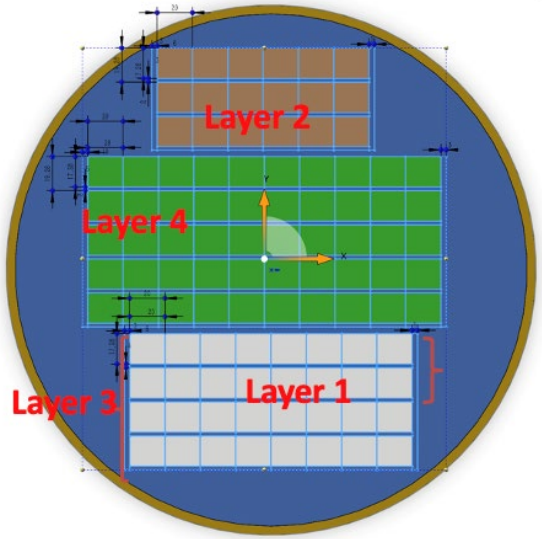
VTX-Data Link







- VTX scheme: Inner 4 layers stitching, with 1 typical double-sided ladder (layer 5&6)
- Bkgrd rate @50MW @Higgs with safety factor 1.5
- Assume RSU@stitching = ladder chip = 1024*512 matrix, then data rate for the innermost layer for a "chip" is 2Gbps, other layers according the bkgrd ratio
- Inner 2 layers needs 2 fiber chns for each row, due to the high data rate
  - possible to merge into less optical MTX interfaces
- In total 88 fibers = 6 BEE Brd = 1 Data Crate

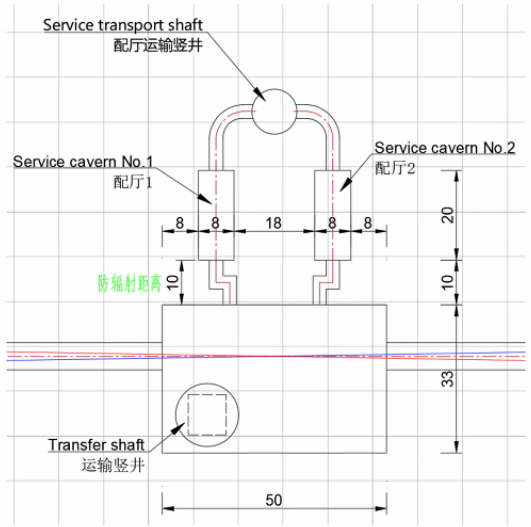


From Zhijun

Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8（2 fiber chns）
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12（2 fiber chns）
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25

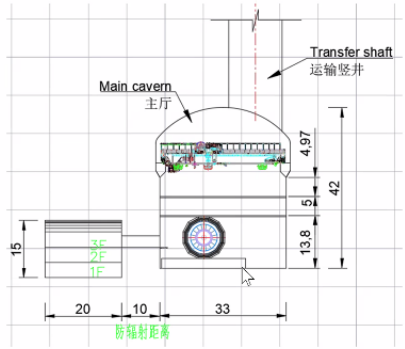
探测器地下大厅设计：

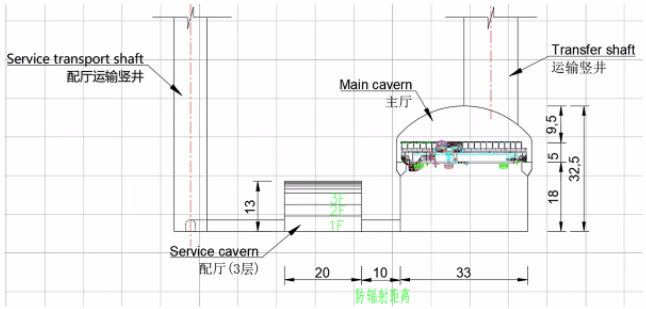
其它比选方案



俯视图

主厅跨度：33 m
高度：32.5 m 和 42 m





侧视图

JUNO根线缆及系统内线缆安装费用参考：

1）电子学内（最多12人）包括20000根电缆桥架，安装：348万

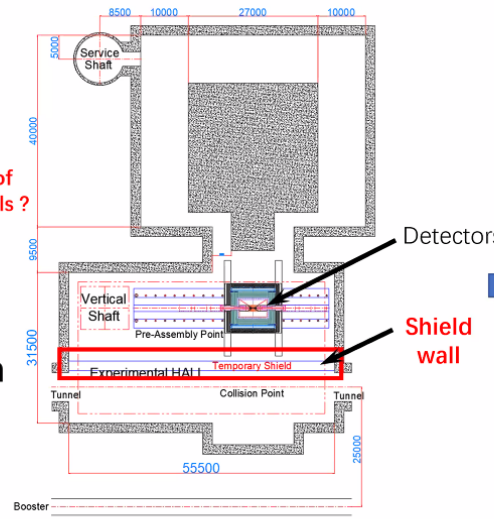
2）实验大厅7000线缆（最多20人）：360万

3）CEPC共计87,984根电缆及光缆，估计约1.5倍JUNO安装费，约1000万

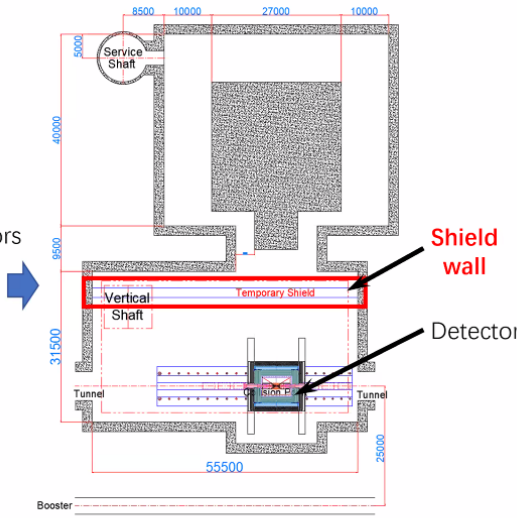
2. 探测器辅助设施及布局

How to make full use of temporary shielding walls ?

Optimization
Layout ?
Size ?



Pre-Assembly Point layout



Collision Point layout