DAQ System for CEPC Detector

On behalf of CEPC Detector TDAQ group

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2025.6.17 Barcelona

CEPC 2025 International Workshop

Outline

\diamond **DAQ**

- Requirement
- Architecture design
- Software (Radar) development
 - > V2: ✓ implemented features
 - > V3: **⊠**ongoing research activities
- ♦ DCS
- ♦ ECS

Summary

Overall Design of TDAQ and Online



CEPC Detector Requirement – Data Rate



Table 12.4: Trigger rate estimation table for different run conditions. The physical event rate is introduced in Section 12.1.1.1. The detailed readout rates of each sub-detector are shown in Table 12.12.

Operation phase		Ι		п	III
Condition	Higgs	Z (12.1 MW)	W	Z (50 MW)	$tar{t}$
Non-empty bunch crossing rate(MHz)	1.34	12	6.5	39.4	0.17
Luminosity $(10^{34}/cm^2/s)$	8.3	26	26.7	95.2	0.8
Physical event rate (kHz)	0.5	10	1.1	40	5.7×10^{-2}
L1 triger rate (kHz)	50	120	65	400	2
DAQ readout rate (Gbyte/s)	49.0	72.8	-	555	-
HLT rate (kHz)	1	20	2	80	1
Raw event size (kbyte)	1453.5	801.1	1500	2042	1000
DAQ storage rate (Gbyte/s)	1.5	16	3	163	1

* Event storage ratio for bkg/phys < 1

- ♦ Readout 50-550 GB/s
- ♦ Storage 1.5-160 GB/s
- Online processing (HLT included)
- Scalable, flexible for possible full software trigger upgrade

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DAQ Architecture Design

✓ Seamless HW/SW trigger compatibility

♦ Smooth upgrade to full-software triggering

Infrastructure Foundation

- Full COTS(commercial-off-the-shelf) hardware
- ◊ RADAR software framework
- ♦ Heterogeneous *computing platform*
- Two-stage HLT design
 - ♦ 1st: fast reconstruction
 - ♦ 2nd: full reconstruction with online calibration

Decoupled scheme

- Memory/disk buffering pools
- Environment-agnostic compute
- Online integration of offline algorithms



Streaming Readout Framework – Radar

heteRogeneous Architecture of Data Acquisition and pRocessing

Version	Deployment	Data rate	Trigger mode	Key updates
V1	LHAASO	~ 5 GB/s	SW Only	- Baseline implementation
V2	JUNO	~ 50 GB/s	Hybrid	ContainerizedPartial HA
V3 (Dev)	CEPC detector (Future)	~ TB/s	Default HW + Possible SW	Heterogeneous processingFull HA

Introduction to Radar V2

Genera	al-purpose	e distribu	ted fram	ework	D)ata F	low S	oftv	vare: pro	oces	s data	Э
⇔ Tr ⇔ Se	ansport lay ervices – Ka	/er – Zerol Ifka / Zooł	MQ Keeper ba	sed	Re	e ad Out Pl D SPMT	ug Module TT	25	Process Algo Reconstructio	rithm Plu	u g Modul ompressic	es in
Onlin	e Software HT	e: manage TP Interfa	ement & s ace	ervices	C	D LPMT	WP		CCSN C Softv	Online Mo	onitor ger	
Online Services	Configuration Service	Run Control Service	Message Service	Process Management Service	Re	eadout	D	Pata	Data		Data	
	Mes	sage Bro	kers	Process		loquie	D	istribute	ed Framework		Storag	2
Client Interface	Configuration Interface	Run Control Interface	Message Interface	Management Interface			Data Ao	quisitio	n Utility Module	s		
	Data	Flow Sof	tware		Run	ning at	t JUNO	for >	• 0.5y for c	omm	ission	ing

Data Flow Software



- Lightweight structure
- ROS + DA + DP + DS
- Plug-in modules design
- Integrate customized readout / processing modules

DAQ Data Assembly



Assembled by trigger ID or timestamp

♦ HW / SW trigger supported

Oniform processing triggered & trigger-less data

♦ Multi-level assemble – ROS + DA

Online Data Processing

Preprocessing Algorithm Customized algorithm Multi-stage data processing: Waveform Event MM Event Software Trigger Assemble Assemble Data preparation / preprocessing Core event processing > HLT algorithm can be integrated Event Event Data Input **Event Process** Event Output Preparation Compress **Parallel processing** Interface provided MM Event Event **CCSN** Monitor **Plugin algorithm** deployment ... Reconstruction Process Customized algorithm **Core Processing Algorithm CCSN:** Core Collapse SuperNova 2025/6/17 10 **MM:** Multi-Messenger

Data processing is flexible, configurable

Online Software Overview



- ◆ **Centralized messaging topology** → message brokers **decouple** online data flow
- ◆ **Microservices architecture** → Independent & Loosely-Coupled Services
- ◆ Layered component design interface, message, online services and supervisor
- ♦ Kubernetes-Managed Containers → Orchestrated Operations

Online HA Design & Implementation



Failure Detection

Heartbeat Detection

- Inter-Process: Based on ZooKeeper
- Inter-Node: Based on ICMP Protocol

Failover

- Redundancy + Master-Slave Election
- Takeover scheme based on Kubernetes
- Solutions for rapid restart of services

Anomaly detection and recovery fully implemented
 Services recovered within seconds, ensuring overall reliability

Radar V3 – Current R&D

Readout protocol	RDMA research
Dataflow	HA design
Online processing	Heterogeneous computing platform
Online cache	Distributed memory cache pool

Implement RDMA on FPGAs

DAQ readout protocol

• Alt. to TCP for possible software trigger upgrade

Protocol Selection

RoCE v2: low cost, high perf.

Firmware Design: Integrate RDMA Logic with UDP

- RoCE Core: UDP Parsing/Generation
- RDMA Scheduler: RoCE packet Verification & ARP Handling
- Packet Verification: Validates data packets
- DDR4 MIG: Data cache management
- Point-to-point test platform built
- Development status
 - ICMP & ARP
 - RDMA send / write + connection management
 - RDMA recv / read in progress





Dataflow HA Design

- ♦ Goal: Auto-recover + minimum data loss
- ♦ Develop process recovering scheme
 - ◊ Dynamic update
 - ♦ State machine path update
 - $\diamond\,$ Test passed in dataflow
- ♦ Data recovery solutions
 - ♦ From backup node | From upstream node

[ONLINE HA] ● Implemented in Radar V2
 [DATAFLOW HA] ◎ Developing
 → VISION: Radar v3 → Full HA DAQ framework



Processing - Data Assembly

- L1 trigger ID based event building
- Batch pack for parallel processing
 - ♦ ↑ GPU utilization
 - ♦↓ TPC data overlap

trigger 0							
	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC
trigger 1							
	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC
trigger 2	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC
trigger 7							
	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC
trigger 8							
	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC
trigger 9	Vertex	ITK	ОТК	ECAL	HCAL	Muon	TPC

34us

Processing - Heterogeneous Computing Platform

Support HLT or full-software trigger mode

- ♦ Heterogeneous scheduler
 - ♦ Balanced Loading: schedule across devices
 - ♦ Data-aware Strategy: co-locate dependent tasks
 - Oev-Friendly: unified memory management

♦ Compatibility Matrix

Туре	Supported	To be supported
Buffer	Disk	Shared Memory • Memory Buffer
Protocol	ТСР	RDMA
Compute	CPU • GPU	FPGA
Memory	CPU • GPU	FPGA

Status: V1 Released • Internal Validated

	# / cepc-online-computing-platform	View page source
	cepc-online-computing-platform	n
	Welcome to the CEPC Online Computing Platform document	itation!
	This Online Computing Platform serves as a framework for o	nine algorithm development and
	execution for CEPC. It is also an part of the Radar (A kind of	online processing framework) v3.0.
ithm	If you have any quesition or suggestion, please contact Zhan	gXu(zhangxu00@ihep.ac.cn).
n	HearCuida	
	UserGuide:	
	Introduction	
	Framework	
	Algorithm	
	• VTX	
als	• ITK	
	* TPC	
	• OTK	
	♦ ECAL	
	Build Project	
	 Single Mode 	
	Online Mode	
	Run project	
	Add New Algorithm	
	 A Simple Example 	
	 An Advanced Case 	
	 Suggestions 	

P main ~ online-computing-platform /	+ ~	History	Find file	Edit ~	Code ~	
add new devicetype in funct.cu				46f97a	98 🚯	
Name	Last commit			La	st update	
🖆 algs	add new devicetype in func1.cu			5	days ago	
🖿 algs_only_cpu	init version			2 w	reeks ago	
🗅 buffer	using global marcro, finish run			1 n	nonth ago	
E device_interface	add new devicetype in func1.cu			5 days ago		
🖹 device_manager	a temp version, add device scheduler	a		2 weeks ago		
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Clang-format	first version 202	5/6/17		2 m	onth 700	

MemIO – Distributed Memory Cache Pool

□ Why

- > Decoupling
- \rightarrow Dynamic Readout + Heterogeneous Compute
- Memory Aggregation
 - > Speed >> Disk
 - > Online compute focus: Throughput > Capacity

Core advantage

> High Tput | High Eff. | High Rel.

Choice

- > Trade-off: Perf. + Avail. VS Cost
- Strategy: OR/AND Buffers

Research Progress: V1 ✓ | LHAASO Test 🛣 ► Next: RDMA 🕕 CPU | MemFS 🎸 | Optimize



Detector Control System: Requirement

Maximize experimental efficiency & data quality via stable, reliable, secure operation



Table 12.16: Summary of detector control and monitoring quantities

Equipment	Channel Number	Control and Monitoring Items	Total Count
AC-DC Crate	55	Switch, voltage, current, etc., about 6 items	330
AD-DC Channel	550	Switch, voltage, current, etc., about 6 items	3300
FEE Power Crate	390	Switch, voltage, current, etc., about 6 items	2340
FEE Power Channel	17696	Switch, voltage, current, etc., about 6 items	106,176
FEE Board	27984	Voltage, current, temperature, etc., about 10 items	279,840
BEE Crate	110	Switch, fan, status, etc., about 10 items	1100
BEE Board	1018	Switch, voltage, current, etc., about 6 items	6,108
Trigger Crate	20	Switch, fan, status, etc., about 10 items	200
Trigger Board	150	Switch, fan, status, etc., about 10 items	1500
HV Crate	91	Switch, fan, status, etc., about 10 items	910
HV Channel	18694	Voltage, current, status, etc., about 6 items	112,164
Gas	1	Flow control, humidity, etc., about 30 items	30
Environmental	3568	Temperature, humidity	5448
Total			~520,000

Detector Control System: Design



Key function modules

- Automated Process Control
- Real-time Monitoring & Alarms
- Detector safety interlock
- Remote Access





Experiment Control System

Deliver secure, efficient experimental control in demanding experimental environments



Scope	Centralized, higher-level than DCS
Integration	DCS + DAQ + other sub systems
Safety	Fault detection + Auto-recovery
Automation	AI analytics + Resource control
User Experience	Intuitive GUI + Unified access

Experiment Control System: Design

Central control software architecture



ECS user interface framework design

ML-based Anomaly Detection

More real-time and automatic monitoring, ensure the experiment efficiency



- Realtime anomaly detection system
 - ♦ Unsupervised Model: Autoencoder
 - ♦ Supervised Model: Neural Network
 - ♦ Model training & optimization
 - ♦ Integrated & tested with Radar

Model	Recall	Prec.	
Autoencoder	~97%	~88%	
Neural Network	~99%	~99%	
Next: Multi-m	odel for	scenarios	* Test with S

Provided a solution for real-time anomaly detection, has been validated in DAQ workflow

Al-based Intelligent Assistant

More efficient and intelligent information integration and interaction

A RUNNING., Stop

♦ INFRASTRUCTURE

- ✓ Private KB & LLM Deployment
- ✓ Stable Query API

♦ RAG INTELLIGENCE LAYER

- RAG-Powered Assistant
 - ♦ Efficient Archive/Retrieval
- ✓ RAG Evaluation Framework
 - ♦ RAG chain tuning

♦ Application

Auto-Anomaly Diagnosis Engine

► Next

- ♦ Multi-modal extension
- ♦ Anomaly Detection Integration

🗩 ТАО-СНАТ

g^{er} A chatbot powered by custom RAG and Sentence Transformers

How can I help you?

GU 8102 channel 93 TimeStamp Error CurrentTime 1995850096117251 LastTime 199585177092901 interval 1673975650 CurrentOverflow 2 LastOverflow 2 GCU 8127 channel 111 TimeStamp Error CurrentTime 199748364552212 LastTime 1997636098708708097 interval 152453184785 CurrentOverflow 2 LastOverflow 2, and the values of multiple GCUs are zero. Answr in Enelish.

According to the context, the TimeStamp Errors for GCU 8102 channel 93 and GCU 8127 channel 111, along with multiple GCUs showing zero values, may be due to: "Overflow issues." The CurrentOverflow and LastOverflow values of 2 indicate possible counter overflow, causing timestamp inconsistencies. "High-Voltage Data Acquisition Problems." After applying high voltage, multiple GCUs may lose data, with timestamp disorder. This could be due to overflow (counters not incrementing properly). Suggested actions: 1. Contact relevant experts. 2. Shut down the high voltage immediately and stop data acquisition. 3. Review configuration files and DCS data (e.g., HVU power, temperature). 4. Restart the low-voltage power supply and attempt data acquisition again. "Flasher Situations." The Flasher occurs (possible) indicated by increased DAQ trigger rates (elevated GCU DCR status): - Check the DAQ trigger rate is rising... Monitor the GCU DCR status, as Flasher conditions typically cause widespread DCR increases. - For global DCR elevation, shut down high voltage, stop data acquisition, and contact operations personnel. "Summary:" First, shut down the high voltage, inspect configuration files and DCS data, and restart the low-voltage power supply before attempting data acquisition again. If problems personnel. "Summary:" First, shut down the high voltage, inspect configuration files and DCS data, and restart the low-voltage power supply before attempting data acquisition again. If problems personnel investigate DAQ trigger rates and GCU DCR status, as personnel investigate DAQ trigger rates and GCU DCR status, and engage operations personnel integrations personnel integrations personnel integrations personnel integrations personnel integration and contact operations personnel." Summary: "First, shut down the high voltage, inspect configuration files and DCS data, and restart the low-voltage power supply before attempting data acquisition again. If problems personnel increases and GCU DCR status, and engage operations personn

请输入你的问题...





Online/Dataflow

Software Information

Text Information

Anomaly Diagnosis Scheme

Interaction interface display



Finished baseline technical design for DAQ & DCS & ECS

A scalable and flexible design

- Work in different directions is progressing
- Welcome to join us

