# DRD6-Calo

# SiW-ECAL Status and Prospectives

*Vincent Boudry*

Institut Polytechnique de Paris

***CEPC EU WS 2025, Barcelona, 17/05/2025***

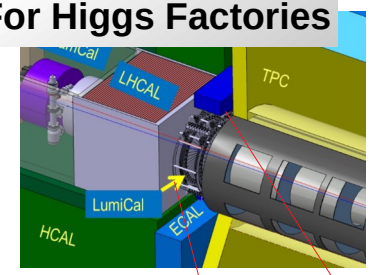
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

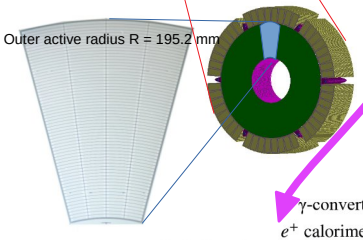
NUCLÉAIRE & PARTICULES

# A Map to High-Granularity Calorimeter Prototypes

## FCAL for ILD, LUXE

**For Higgs Factories**





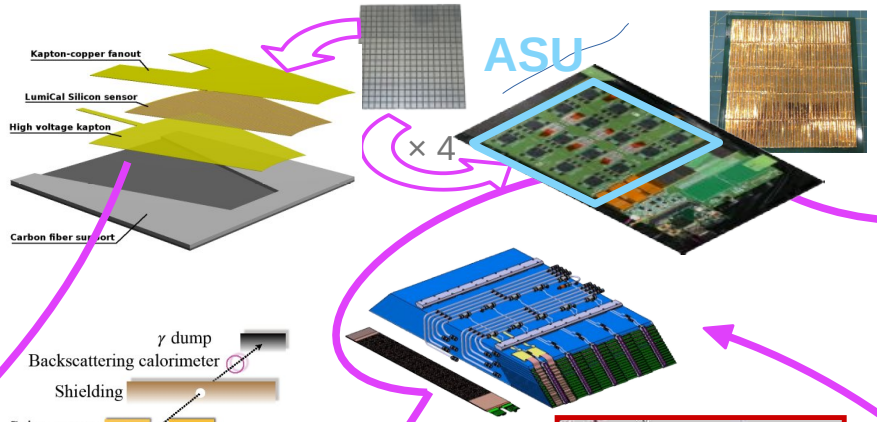


**Non-linear QED**

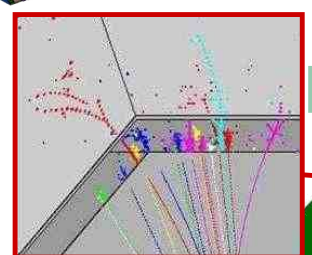
## LUXE, SiW-ECAL, ScECAL for ILD

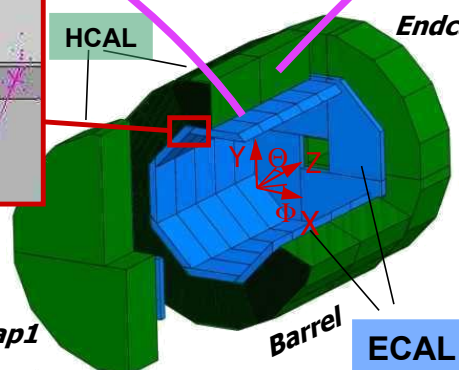
Si 5×5 mm²

Sc 5×50 mm²

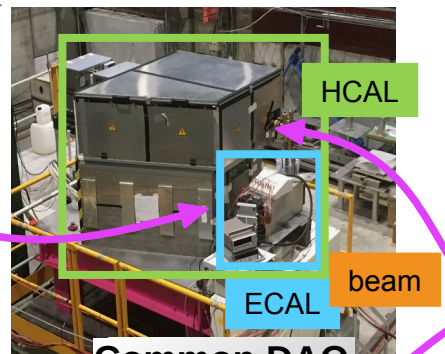




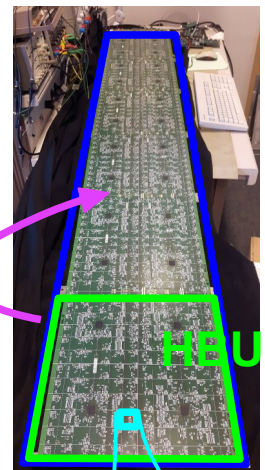



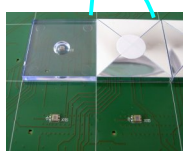



## AHCAL for ILD




**Common DAQ**



Scint 3×3 cm²

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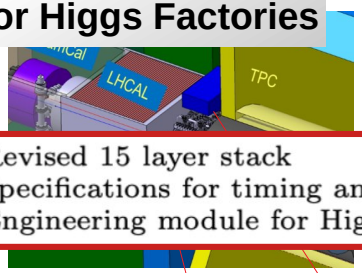
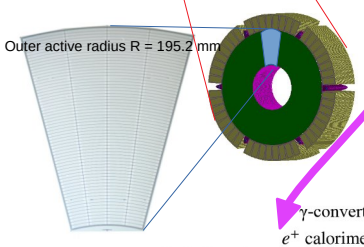
**For Higgs Factories**







**Non-linear QED**

## LUXE, SiW-ECAL, ScECAL for ILD

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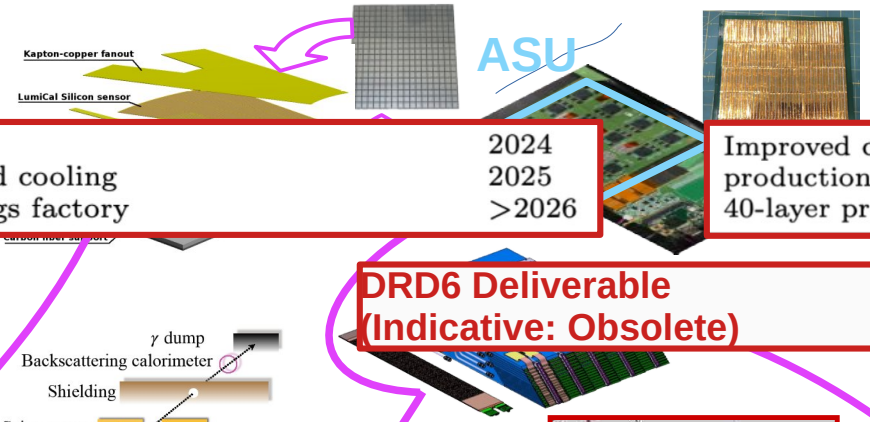
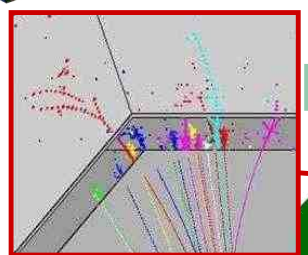
Sc 5×50 mm²

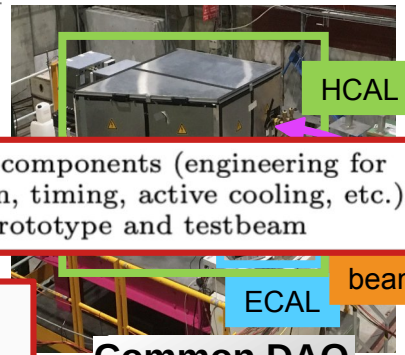



| | |
|---|---|
| Revised 15 layer stack | 2024 |
| Specifications for timing and cooling | 2025 |
| Engineering module for Higgs factory | >2026 |

**DRD6 Deliverable (Indicative: Obsolete)**

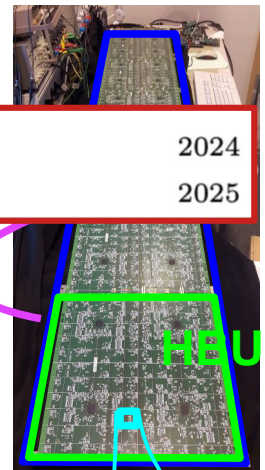


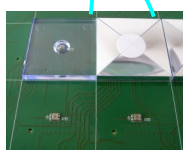
## AHCAL for ILD



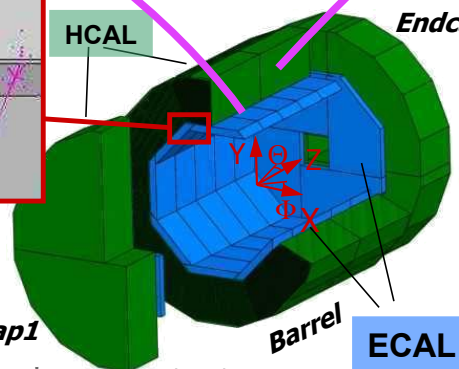

| | |
|---|---|
| Improved components (engineering for production, timing, active cooling, etc.) | 2024 |
| 40-layer prototype and testbeam | 2025 |

**Common DAQ**



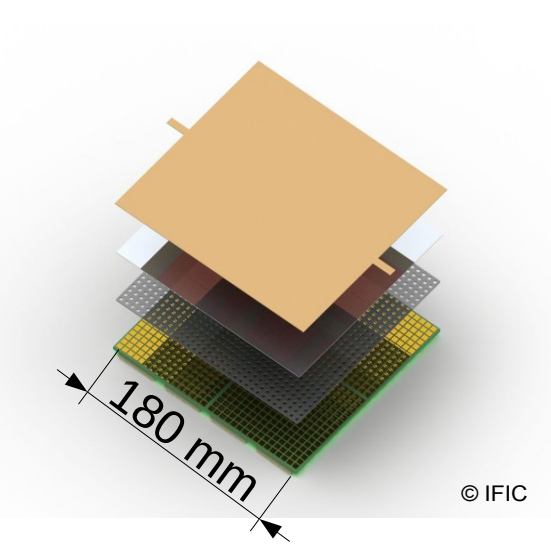



Scint 3×3 cm²




**ILD**
**CLD**

# SiW-ECAL Active Elements

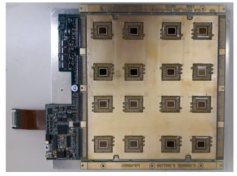



## Base element of SiW-ECAL

- Continuous design improvements
  - Noisy-cell fraction ↘
- Delamination issues in 2022
  - New hybridization process needed

**FEV10, 11, 12**

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014



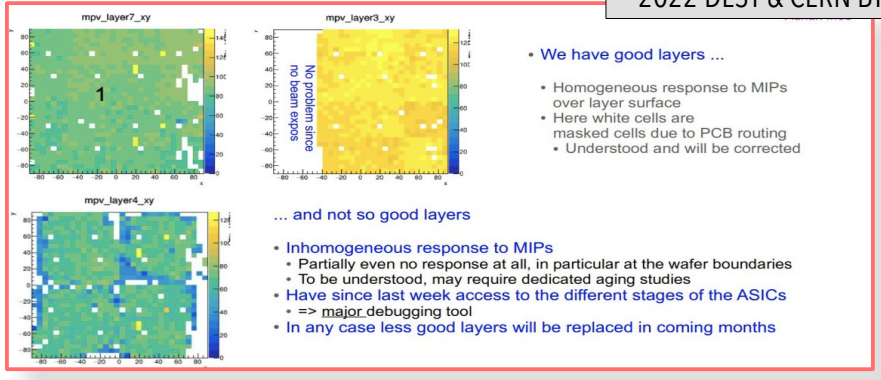
**FEV-COB**

- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

**FEV13**

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

2022 DESY & CERN BT



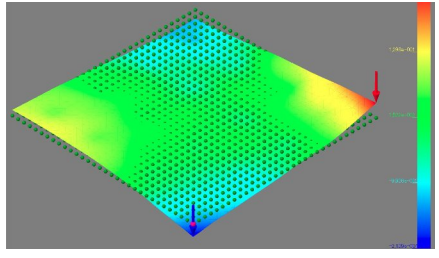

See R. Poeschl's presentation at the AIDAi meeting, March 2024 for more details

# Hybridization studies (2024): How to assemble silicon sensors & PCB ?

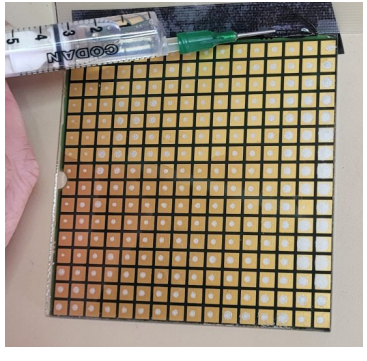
## Revisiting gluing (IFIC, IJClab, DMLAB)

- PCB metrology
  - Bef. & After curing & soldering
- Glue formula & preparation
- Gluing methods
  - Robot
  - Stencil
- Reenforcement
  - Filling glue
  - Adhesive films

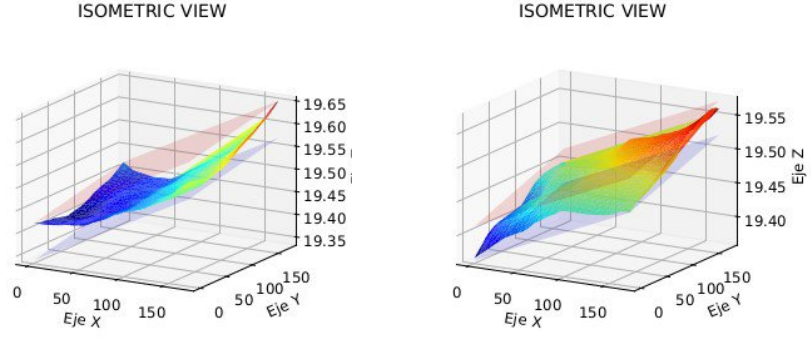
**IJClab** (méca)



Conductive glue + filling (~invisible) on a glass plate



## Flatness of PCB




Same PCB before / after 10-day dry storage


Measurements by C. Orero, IFIC

Puncturated adhesive film (**DMLab**) + conductive glue dots

# Assembly chain:

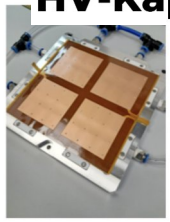
## Metrology of PCBs

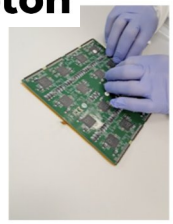
IFIC INSTITUT DE FÍSICA CORPUSCULAR

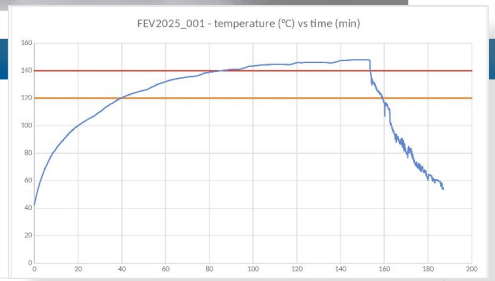
▷ **We could not do conclusive metrologies of the PCBs upon reception**

- Small differences between FEV2.0 and 2.1 and w/ w/o components which make the tools available not suitable… we aim for precision mechanics, we require detailed mechanics models and designs
- At arrival + after drying, requires at least 1 month of time for the full process. → so we decided to dry them before having the definitive tooling (which took some time to be produced)

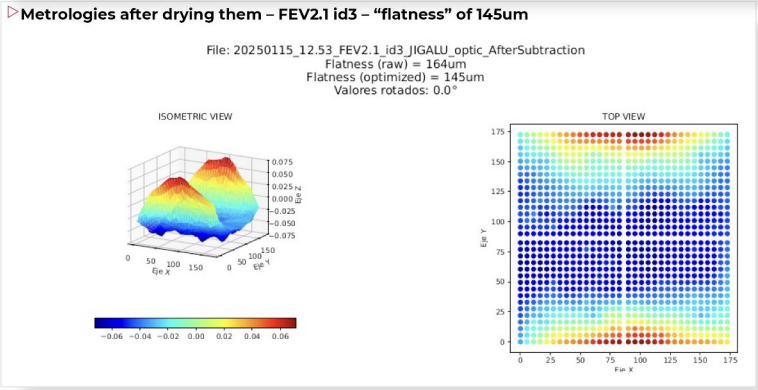
## HV-Kapton



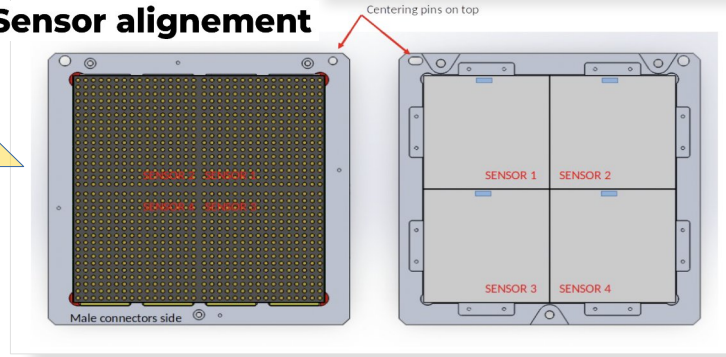





▷ **Metrologies after drying them – FEV2.1 id3 – "flatness" of 145um**




## Sensor alignement




PROCEDURE - 3D robot and precifluid v0.odt

PROCEDURE - CALICE ASU gluing_alignment v0.odt

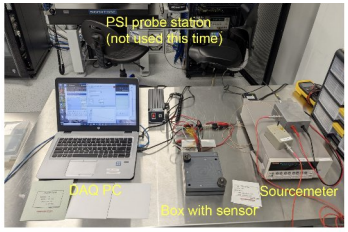
PROCEDURE - CALICE ASU gluing v0.odt

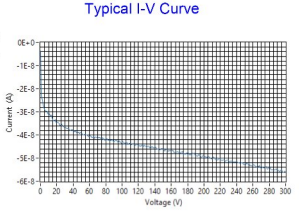
PROCEDURE - H20E preparation v2.odt

PROCEDURE - HV-K… to ASU v0.odt

Sensor and electronics cleaning

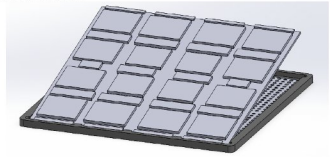
## Sensor characterization

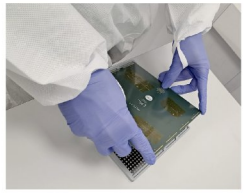


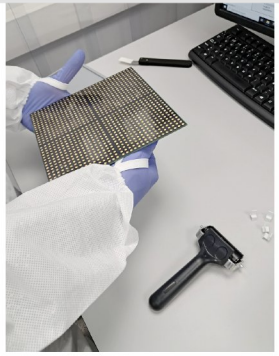



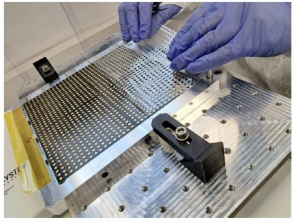

- Reasonable I-V curve though leakage current ~ factor two lower than in HPK data sheet
- Tests allow to validate that there is no major problem with sensors

J. Jeglot, A. Torento, R.P., (R. Cornat)



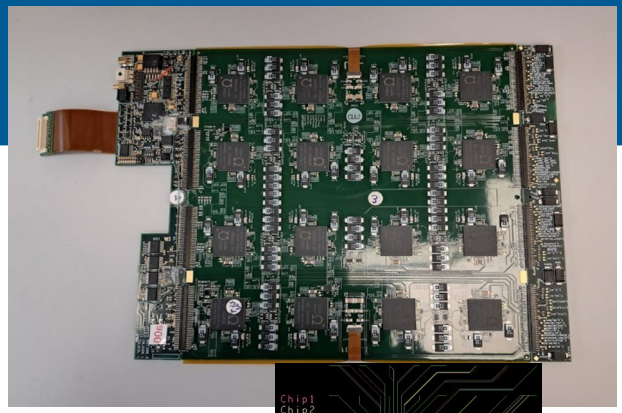






## 3M tape

# New (ultimate?) FE boards (2023-24)

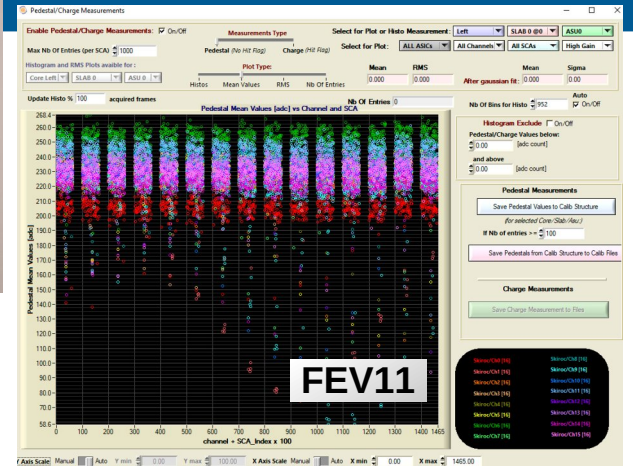



## Improvements:

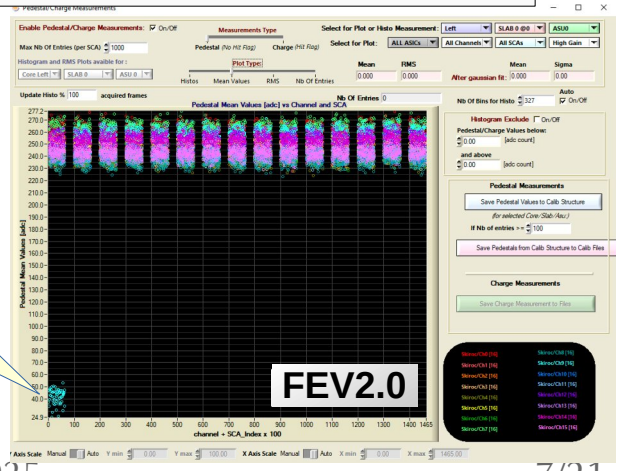
- Power distributions
  - Local LV power regulation: LDO's
  - Local HV filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing

## Status:

- Noise uniformity dramatically improved (ex: outliers in thr. / 20)
- version 2.1 produced
  - 4 cabled, 2nd metrology, 2 equipped with sensors (Fev'25)



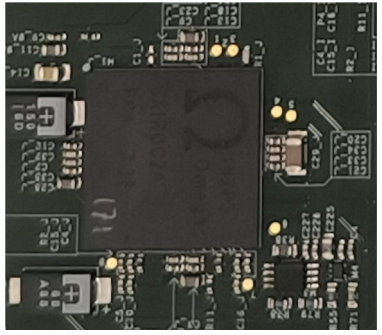

Pedestal measurements vs. Ch# + Mem#×100)

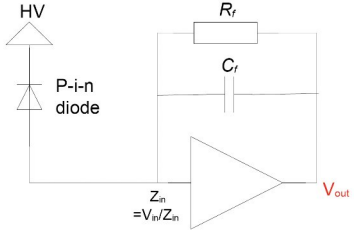



SIngle channel → the fault on the ASIC/packaging

# Commissioning: Analogue Probes

## Analogue Probes

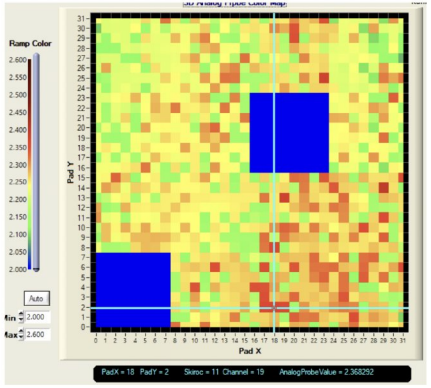





$$V_{out} = V_{in} - I_{in} Z_f$$
$$Z_f = 1/\omega C_f + R_f$$

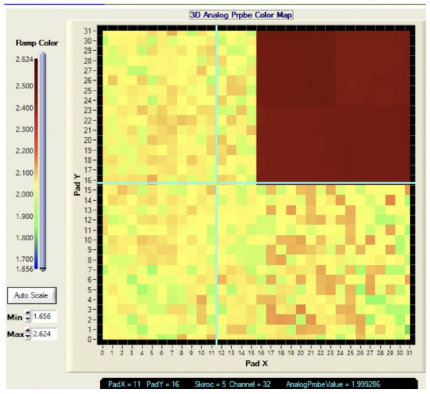
1 value (LV, Channel, …)
→ common line

Two ASICs with short cut diode on input



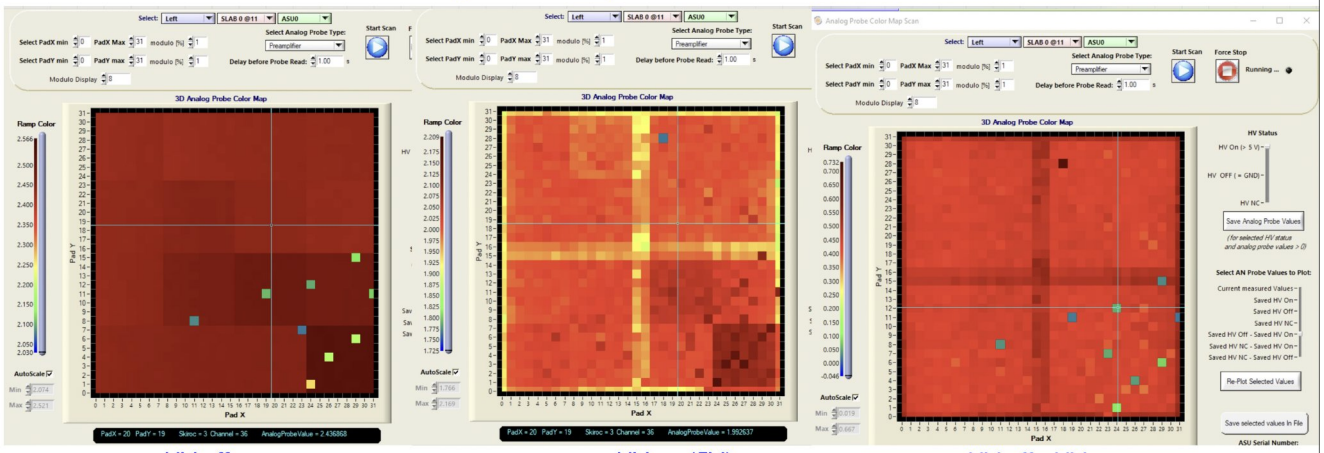
Repaired by Dominique

Badly powered sensor



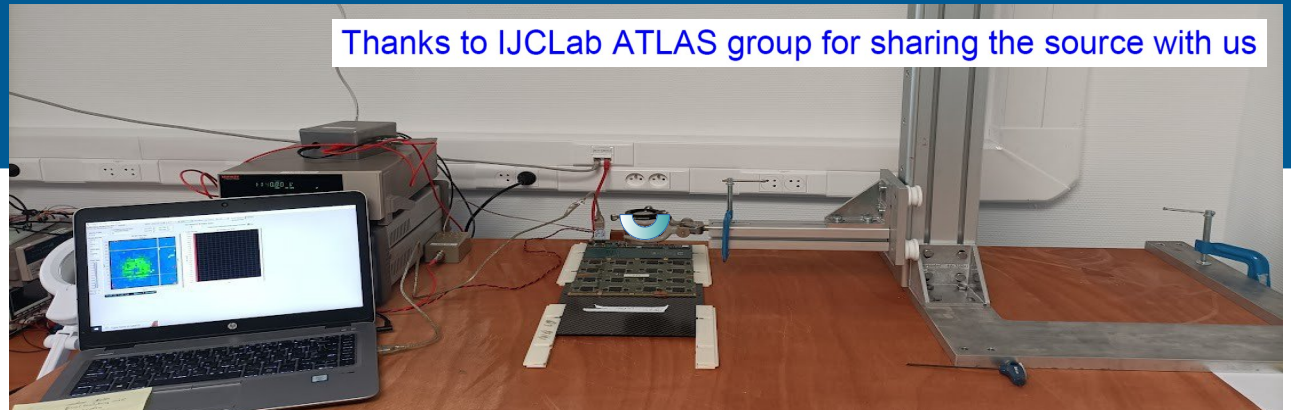
Replugging of HV Connection helped

- Automatic scan over all 1024 cells (~15 minutes)



HV off | HV on (5V) | HV off - HV on

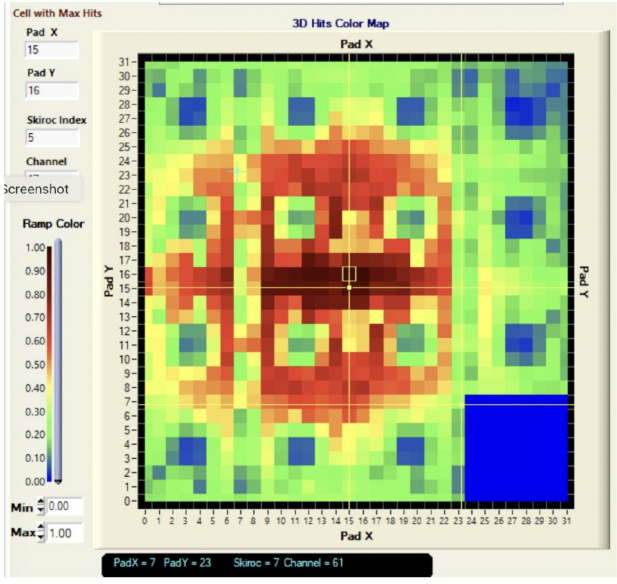
# Commissioning: $^{90}Sr$



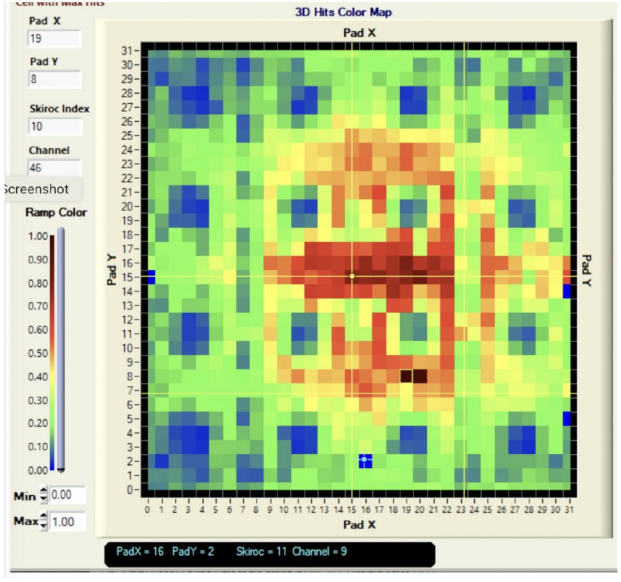

**Tests made one week before BT at DESY**

- 1 faulty ASICs AUS01
- Very few noisy channels

ASU2025_001




ASU2025_002

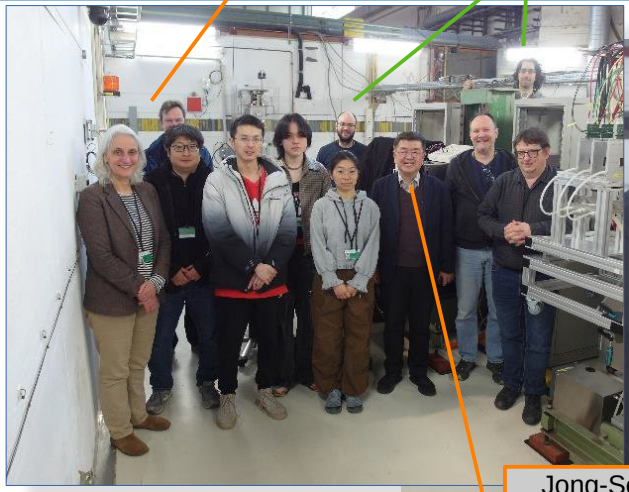



- Source tests allow to validate functionality of all cells (or identify further problematic cells)
- Small blue regions ASIC packaging (-> ok), large blue region one faulty chip

# DESY Beam Tests 2025/03

Ursula Bassler (LLR / DESY)
Dir Zerwas (DMLab)

Antoine Laudrain (DESY)
Jiri Kvasnicka (FZU)



Jong-Seo Chai
(Sewon), Visitor

**1 week 3–10/03/2025**

**SiW-ECAL:**

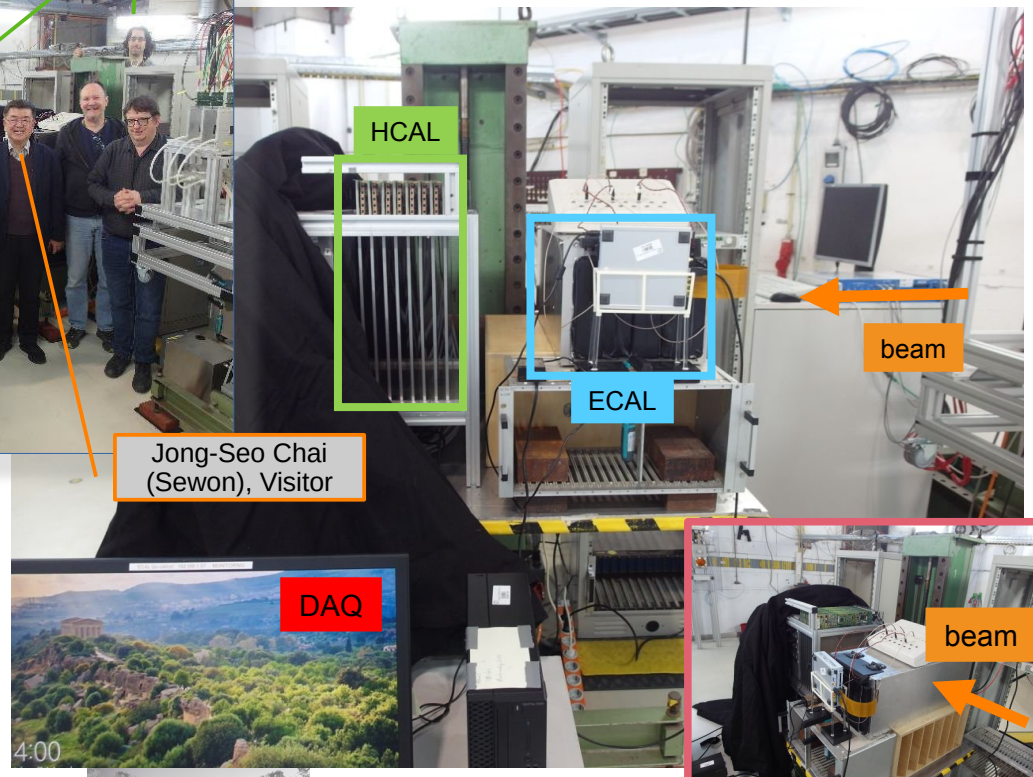
- 2 new ASU FEv2.1
- 1 ASU COB
- No Tungtens

**AHCAL:**

- “Airstack” with 7 short layers

**Running:**

- 3 days ECAL Stand alone
  - ½ d. install + commissioning
  - Positions scans : uniformity & mip/noise resp.
- 4 days AHCAL
  - ½ d install + repair
  - Scans & TDC runs




The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)".

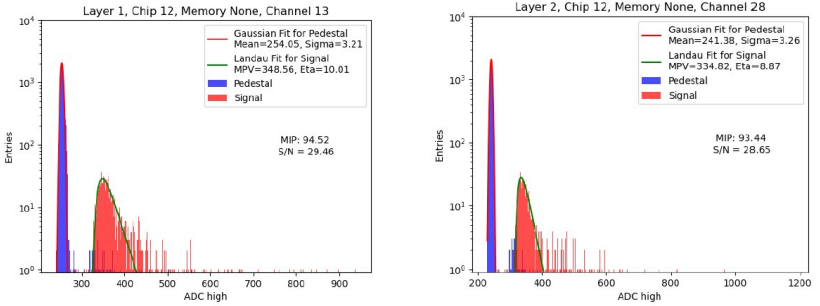
"Toshiko Yuasa"
France Japan
Particle Physics Network
(TYL-FJPPN)

# Some results on the SiW-ECAL

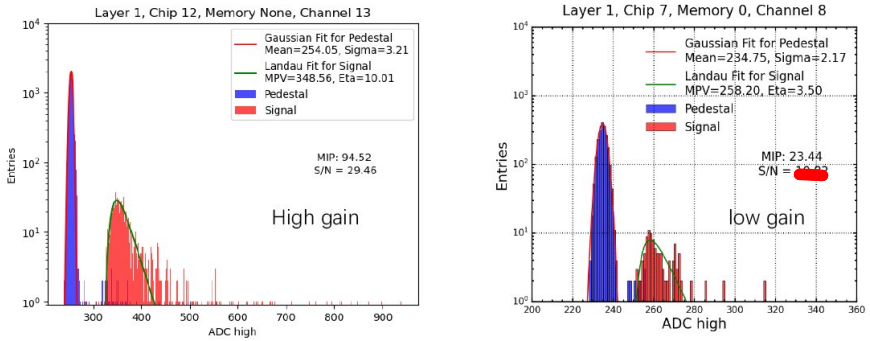
Xin XIA (IJCLab)

## S/N ratio for single channel

- Data: From hold_value scan run (hold value = 130), with high gain of Feedback capacitances
- Pedestal: adc_high[hitbit_high == 0]; Signal: adc_high[hitbit_high == 1].
- For ASU1 and ASU2:
  - MIP ≈ 93 ADC count
  - S/N ≈ 29 (in ADC readout)

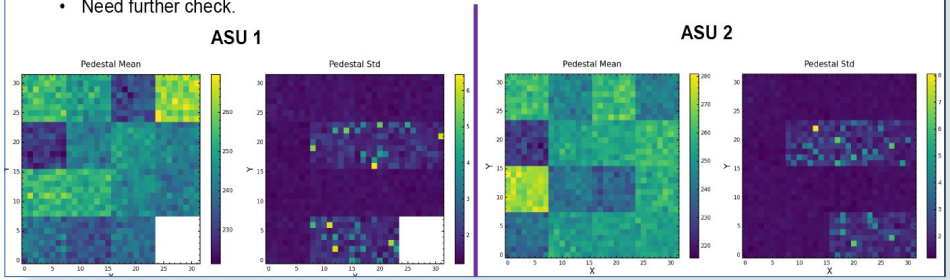



MIP value for different gains of Feedback capacitances




## Pedestal map of pedestal run

- Data: From pedestal runs
- For each channel:
  - Select adc_high[hitbit_high == 0 & badbcid == 0] get the distribution
  - Fit the distribution with gaussian function to get the mean and sigma value
- In each chip, the pedestals are relatively consistent.
- But in some chips, the pedestal sigma is higher than 4 because of two peaks.
- Need further check.




## New FEV2.1 preliminary results:

- High S/N ration (MIP MPV/Noise StdDev) ~ 30 in readout branch
- Run in lower gain mode possible
- Very few cells masked

# Synchronization ECAL–AHCAL

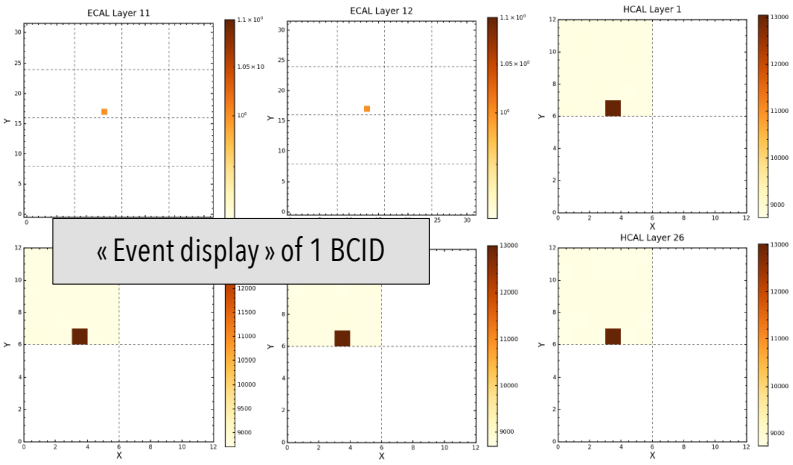
*Aim: consolidate the Digitization, including timing*

## Set-up identical to 2022

- Same setting as in 2022
  - Bunch Clock cycle offsets (BCID's)
  - Reconstructed ΔBCID's OK
  - TDC information being analysed

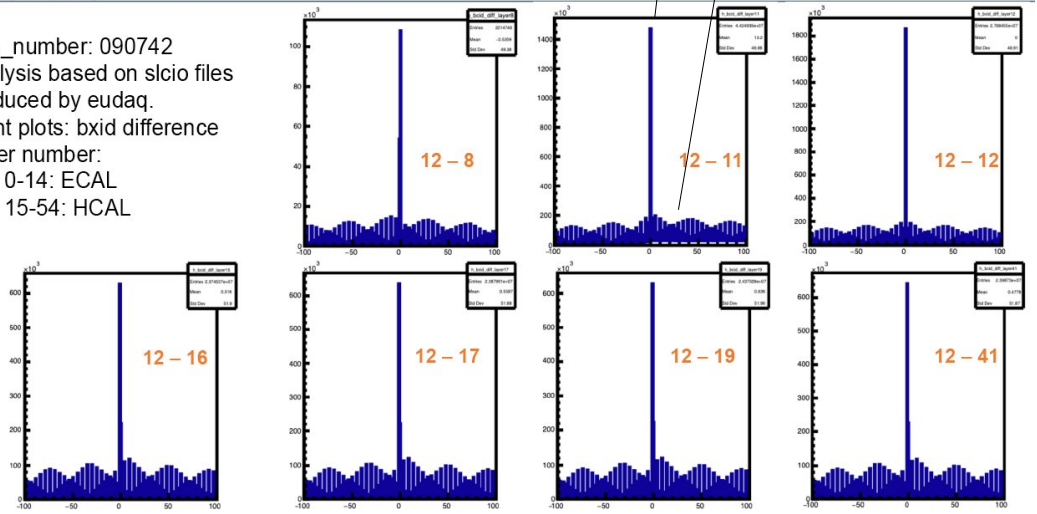
Main BCID
lay. 12 – lay. 11

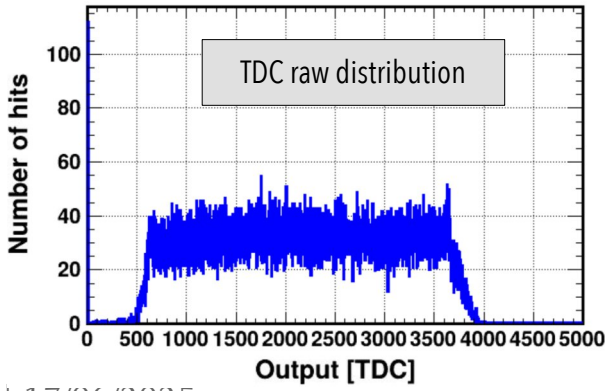
Coincidental events following beam time structure




« Event display » of 1 BCID

- Run_number: 090742
- Analysis based on slcio files produced by eudaq.
- Right plots: bxid difference
- Layer number:
  - 0-14: ECAL
  - 15-54: HCAL

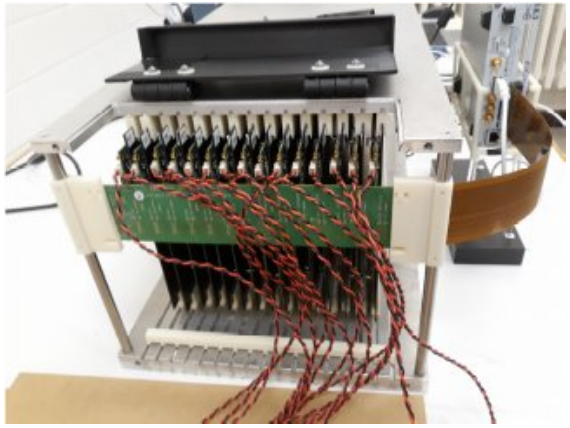


# Building of a uniform SiW-ECAL prototype

**Rationale:**

- Current prototype
  - 4(5) types of PCBs ⊗ 3 sensor thicknesses (320, 500, 625 µm)
  - (un)gluing issues
- Material for 15 ASUs available ➞ full single tower
  - FEV2.1 boards, wafers, components



**Application cases :**
**LUXE@XFEL, EBES@KEK, Lohengrin@ELSA, SHiP?**

- Extreme QED & Dark $\gamma$ searches
- low energy, rates, …
- LUXE: FCAL prototypes ➞ common DAQ Application.
- Could be built from *same cards* in 2×12
  - Needs: sensors (€), (Mech. structure), W

  ⊕ **Will provide operational experience**

# Calice TAU sensors for LUXE

## 90 CALICE sensors received mid November 2023

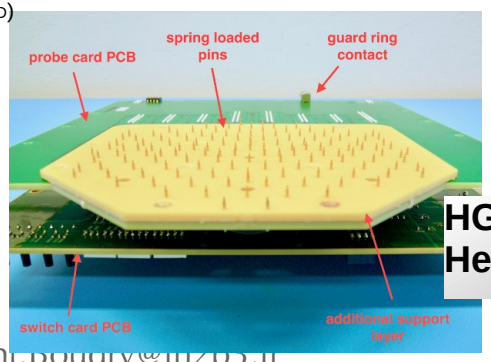
## A probe card was designed and received in November from CERN

(paid by TAU and IFIC).

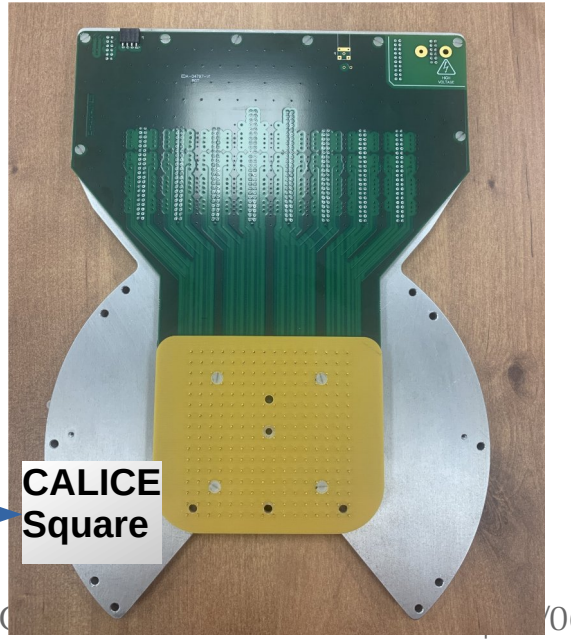
| Parameter | Rating | Unit |
|---|---|---|
| Device type | P+ PIXEL on N substrate | |
| Chip size | 89700 ± 40 x 89700 ± 40 | μm |
| Active area | 88480 x 88480 | μm |
| Chip thickness | 320±15 | μm |
| Number of PIXELs | 256(16 x 16) | ch |
| PIXEL pitch | 5530 x 5530 | μm |
| PIXEL GAP | 10 | μm |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| substrate resistitance | | | 3 | --- | --- | kΩ・cm |
| Full depletion voltage | Vfd | | 15 | --- | 120 | V |
| leakage current(for inner PIXEL*2) | Id | VR=200V | --- | --- | 25 | nA |
| leakage current(for outer PIXEL*2) | Id2 | VR=200V | --- | --- | 100 | nA |
| Number of NG PIXEL | | | --- | --- | 10 | ch |

System needed for electrical sensor characterisation in prototyping phase and for quality control in mass production (IV, CV, $V_{BD}$, $V_{FD}$, $C_{FD}$)




HGCAL Hex

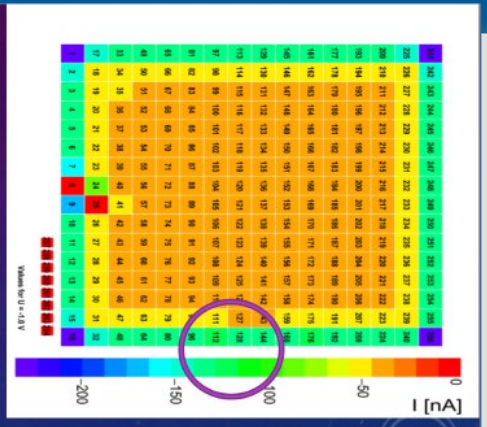


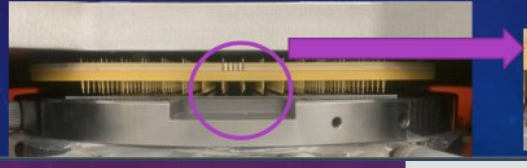
CALICE Square

# Test procedures

## DATA TAKING

- 1st step : contact test to be sure all the pads are touching the probe pins. Takes few minutes
- 2nd step IV test.
- 3rd step CV test.
- We are adding the following steps :
  - Rotation of the sensors (90 degrees)
  - Contact test
  - IV and CV for the missing pins



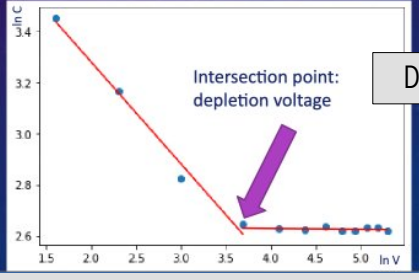
Leakage current

## DEPLETION VOLTAGE

- It is possible to extract the depletion voltage from the CV measurement; the capacitance can be modelized by:

$$C_g = A\frac{\varepsilon_{Si}\varepsilon_0}{w} = \begin{cases} A\sqrt{\frac{\varepsilon_{Si}\varepsilon_0 eN_d}{2V}} & for\ V < V_d, A: pad\ area\ Nd: number\ of\ donor, V\ bias\ voltage \\ A\frac{\varepsilon_{Si}\varepsilon_0}{w_m} & for\ V > Vd, w_m\ max.\ depletion\ width \end{cases}$$

- So if we take the log of Cg, we should obtain two lines. The intersection of these lines is giving the depletion voltage

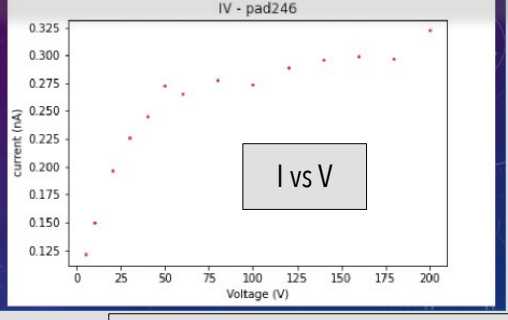



Depletion V

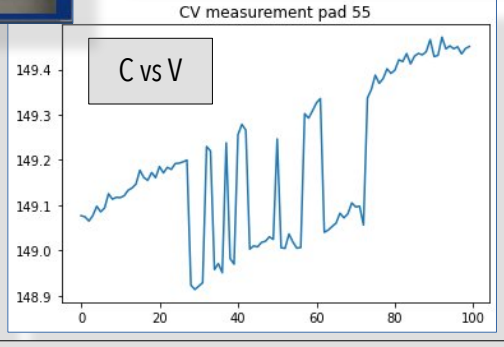
## IV MEASUREMENT

Checked the influence of different parameters: delay between measurements, delay between voltage change,...

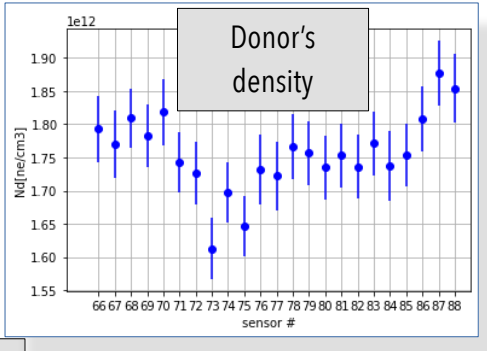
System tuned




I vs V



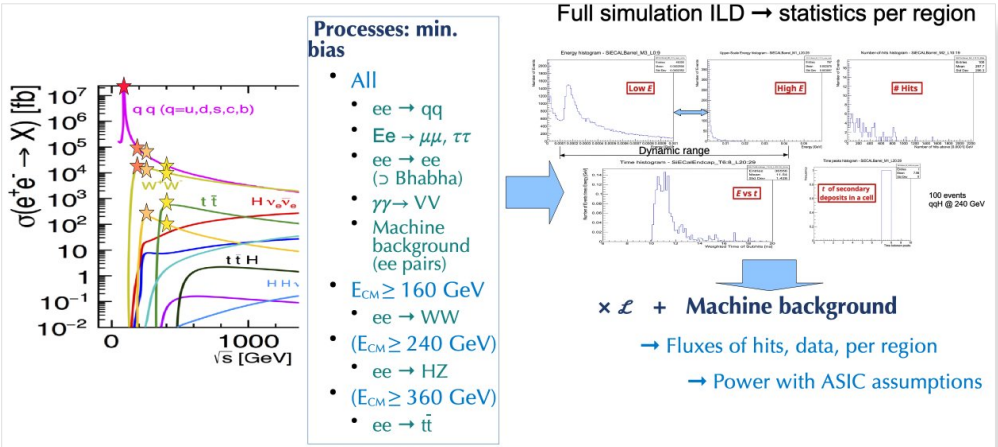

C vs V




Donor's density

For details, see Yan benhammou's presentation at the 3rd AIDAi meeting

# Fluxes in Calorimeters

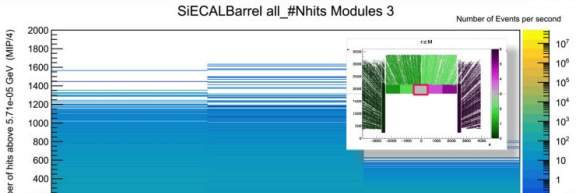



## Take Home:

- Even at Z peak power dominated by pre-amp (↔ conversion power in negligible)
- Tool is there, missing:
  - Digitization (easier way in Key4HEP ?)
  - Mapping needs to be adapted for each calorimeter readout topology

## Results : Rates in Silicon ECAL Barrel, Central Module vs depth

Similar results for ScECAL, SDHCAL, AHCAL




Distributions of the number of hits crossing (MIP/4) energy threshold of all the physics processes and machine background at 91.2 GeV (FCC-Z4)
The $z$ scale is the number of event/s

From the $\langle f_{Nhits} \rangle$ in one region one can extract :
- The data rate, knowing the number of bytes per hits (here 7 as a landmark)
- The occupancy, knowing the number of cell in the region.
- The power dissipated on elec. power (here for SKIROC2 like chip)

| M3 all staves | L0:9 | L10:19 | L20:29 |
|---|---|---|---|
| Average #hits/s | 302E+6 hits/s | 65E+6 hits/s | 8E+6 hits/s |
| Max | 2000 hits/event | 2500 hits/event | 1000 hits/event |
| Data rate | 2,11E+9 B/s | 458E+6 B/s | 54E+6 B/s |
| Ncells | 4 026 764 | 3 767 273 | 3 378 036 |
| Occupancy/BX | **1,4 E-06** | **3,3 E-07** | **4,3 E-08** |
| Base power/W | 18,2 E+03 | 17,1 E+03 | 15,3 E+03 |
| Conversion power/W | 271,4 E+00 | 58,9 E+00 | 6,9 E+00 |
| Total power/W | **18,5 E+03** | **17,1 E+03** | **15,3 E+03** |
| % conv. | 1,5 % | 0,3 % | 0,05 % |

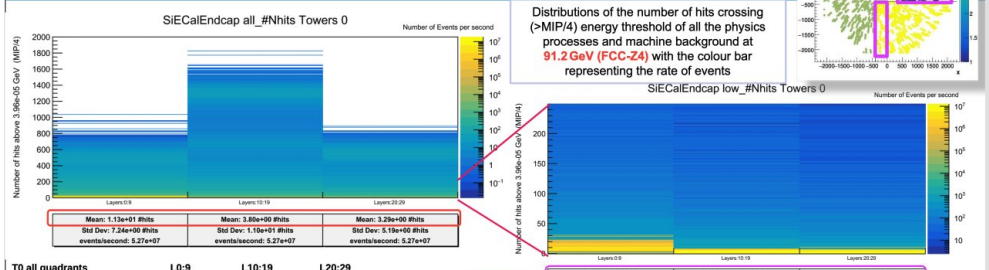
| | |
|---|---|
| cell size | 5,5 |
| Bytes/hit | 7 |
| powa (W/cell) | 4,5 E-03 |
| powb (J/hit) | 8,7 E-10 |
| Conv & RO E/hit/μJ | 9,0 E-01 |
| Δt/s | 19 E-09 |

- **Most of the hits are in the first third of the calorimeter.**
- **Highest average rates L0:9**
- **Highest max rates in L10:19**

**Note 1** : (still) **preliminary**
**Note 2** : Rates & Power for all M3 modules
→ 8 per module, 10 per layer for 1 slab
→ ~ 50 W/slab

## Results: Rates in SiECAL EndCaps, Tower 0 vs depth

Similar results for ScECAL, SDHCAL, AHCAL




Distributions of the number of hits crossing (>MIP/4) energy threshold of all the physics processes and machine background at 91.2 GeV (FCC-Z4) with the colour bar representing the rate of events

| T0 all quadrants | L0:9 | L10:19 | L20:29 |
|---|---|---|---|
| Average #hits/s | 572E+6 hits/s | 176E+6 hits/s | 147E+6 hits/s |
| Max | 2000 hits/event | 2500 hits/event | 1000 hits/event |
| Data rate | 4.00E+9 B/s | 1E+9 B/s | 1E+9 B/s |
| Ncells | 1,161,775 | 1,161,775 | 1,161,775 |
| **Occupancy/BX** | **9.4E-06** | **2.9E-06** | **2.4E-06** |
| Length/Width | 2496 | | 565 |
| Base power | 5E+03 | 5E+03 | 5E+03 |
| Conversion power | 515E+00 | 159E+00 | 132E+00 |
| **Total power** | **6E+03** | **5E+03** | **5E+03** |
| % conv. | 8.9 % | 2.9 % | 2.45 % |

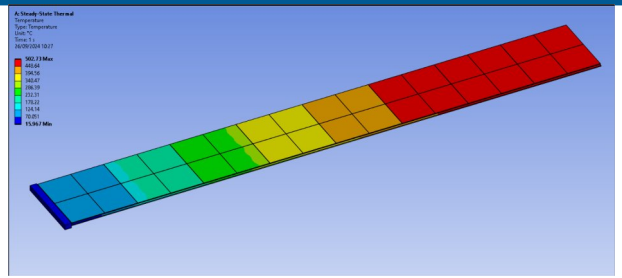
| | |
|---|---|
| cell size | 5.5 |
| Bytes/hit | 7 |
| powa (W/cell) | 5E-03 |
| powb (J/hit) | 870E-12 |
| Conv & RO E/hit/μJ | 0.9 |
| Δt | 19E-9 |

- **Machine background in first layers**
- **High E ee→ee in middle of ECAL**
- **Power driven by the continuous part (Pre-Amps)**

**Note 1** : (still) **preliminary**
**Note 2** : Rates & Power for all T0 modules
→ /8 per quadrant, *10 per layer for 1 slab* → 75W / slab

# ECAL adaptation : flat cold plate, preliminary thermal studies

## Uniform solutions:



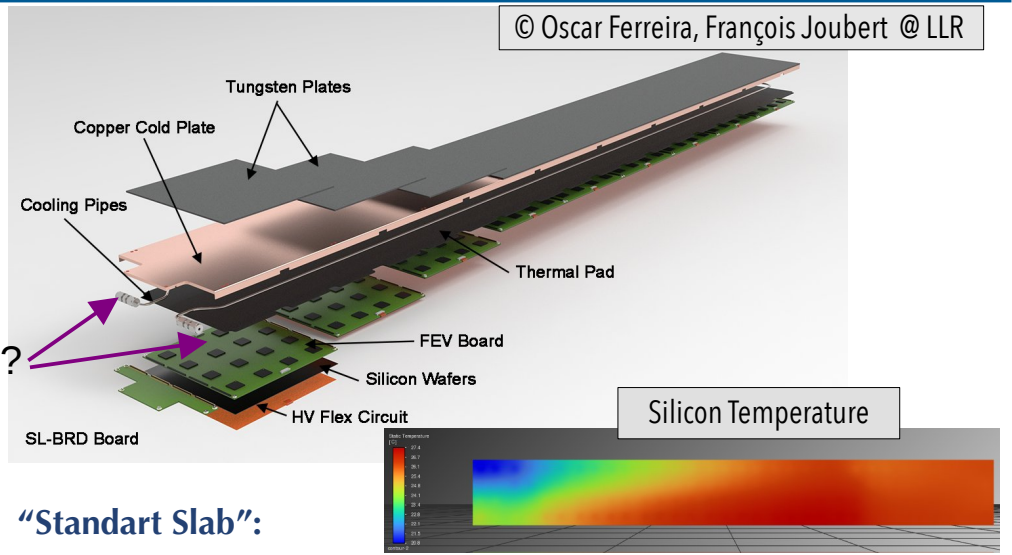
**“Standart Slab”:**

- 8 ASU (1440mm)z, 8192 ch / 128 ASICs
- 100 W

**Passive cooling:** Cu of 2mm (W, C ignored)

Adiabatic, but for heat bridge at the end

**ΔT = 500°C on Wafer surface at $t = \infty$**




Connections ?

**“Standart Slab”:**

- 8 ASU (1440mm), 8192 ch / 128 ASICs
- 128 W (1W/ASIC ~16 mW /ch)

**Active cooling:**

- 4 mm Cu plate with 1/8’’ Stainless Steel Tubing
- 0.2 ℓ/min of water @ 15°C

Adiabatic, but for heat bridge at the end

**ΔT = 6.6C on Wafer surface at $t = \infty$**

## Status:

- Limited flow of water seems enough…
- Now looking into pipe in 4-mm Cu layer
  - Replaces ~1 mm of W
- To be validated on simulations

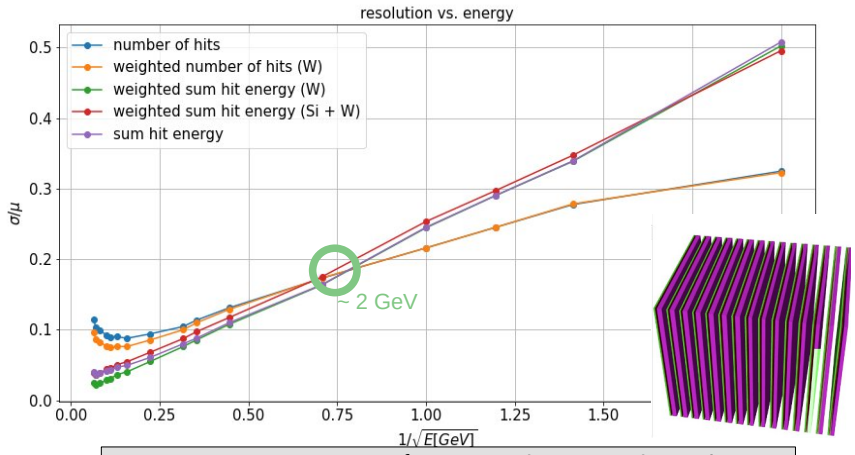
# Re-optimization of the design required (on-going)

## Energy reconstruction methods

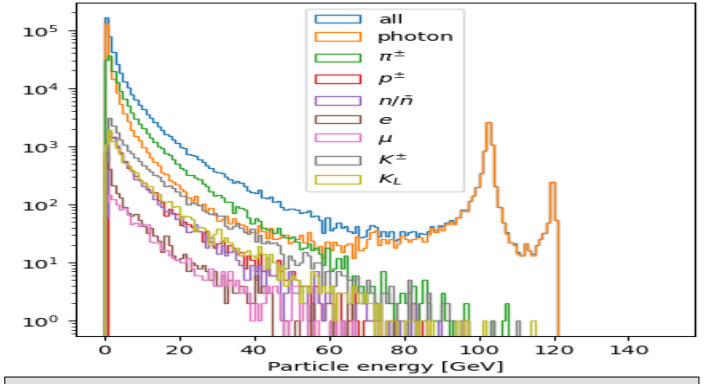
- Counting (Digital) vs Analog
  - Better by counting for Eγ < ~2 GeV
  - How to best combine them ?
  - New methods ?
- $\pi^0$ reconstruction from improved positions
- Timing with 50 ps ? ⇐ 3 years progamme started.

## Re-optimization of sampling :

- Part of W → 4 mm of copper for cooling
- Optimisation for counting at low-E / Start of showers
  Lower the detetction threshold (≤100 MeV ?)
- Work done for LUXE as a method
  (Zarnecki et al, arXiv:2409.19654v1)




SiW-ECAL Prototype of 2022 (15 layers) [Yukun Shi]




Jet Composition at 91 GeV (Hao Liang)

# Recent Progress: CALOROC1C design (Si and ℓAr) – Ωmega

## New ASICs

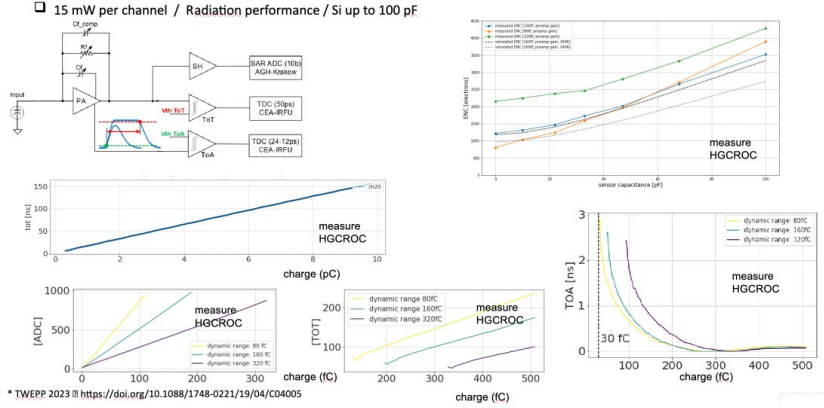
- Based on HGCROC, HKROC

## Compatibility:

- PCB & DAQ work can start with HKROC

### CALOROC1C (based on HGCROC)

- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / Si up to 100 pF



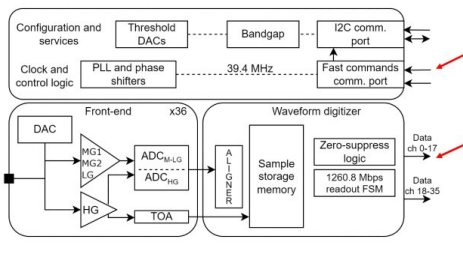

* TWEPP 2023 https://doi.org/10.1088/1748-0221/19/04/C04005

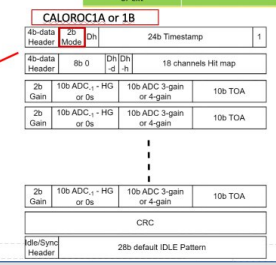
14

### CALOROCs: block diagram and interfaces

- CALOROCs will have the same interfaces (comparable to CMS H2GCROC *):
  - Fast command to dynamically control the ASIC
  - I2C to set the parameters
  - High speed serial links (CernLowPowerSignal compatible)

| Fast commands | Value |
|---|---|
| Idle | 00011 |
| External trigger | 01101 |
| ChipSync | 01110 |
| BCR | 10101 |
| EBR | 11001 |
| Link-sync-ROC or Link-reset-ROC | 10110 |
| Calibration int or ext | 11010 |




* CERN EDMS ➔ https://edms.cern.ch/document/2954073/1

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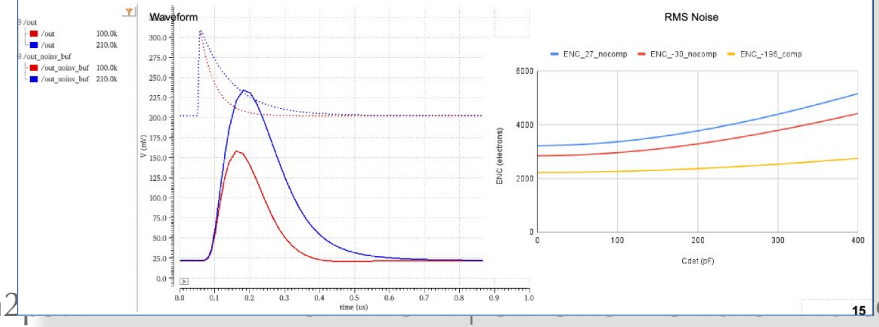
16

### CALOROC1C (based on HGCROC)

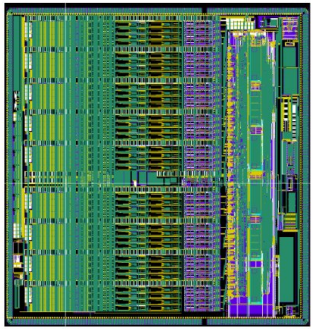
- CALOROC1C will
  - update its back-end (readout streaming)
  - slow down the shaping from 25ns to 100ns




15

### Conclusion

- Conservative **CALOROC1A**:
  - Based on CMS SiPM H2GCROC + SRO
- New **CALOROC1B**:
  - New analog front end
  - Higher dynamic range and input capacitance
  - Same backend (and pinout)
- **CALOROC1C** for Si/LAr detectors:
  - Based on CMS Si HGCROC + SEO
- **All Calorocs share the same backend**
- **All Calorocs will be sent to fabrication this month**



CALOROCs are targeted to include all features + radiation hardness on the first submission

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17

# Conclusions

## SiW-ECAL

- 2 new board produced and put in beam for low-E response
- Preliminary results very promising: OK for production of + 13 new ones
- Will provide input for Digitization code adjustement

## SiW-ECAL Future test:

- **2026**, with full uniform stack of 15 layers, then a long slab
  - Will be used for small experiments (EBES, LUXE, Lohengrin) → operational experience
  - Design will serve a basis for future µ-Electronics

## Coming developments:

- Thin Cold-Plate prototyping + Interfaces (SiW-ECAL)
  - Re-optimisation of **absorbers** + **timing** + `**digital modes**'
- Re-design the PCBs on the basis of new ASICs
  - I2C communication (HGCAL protocols)
- Re-design of DAQ
  - Rates estimations on-going in all calorimeters
- Should aim at scalable prototypes by early 2030's
  - Reminder: 8 years of building for large calos

# Possible planning (FCC-ee)