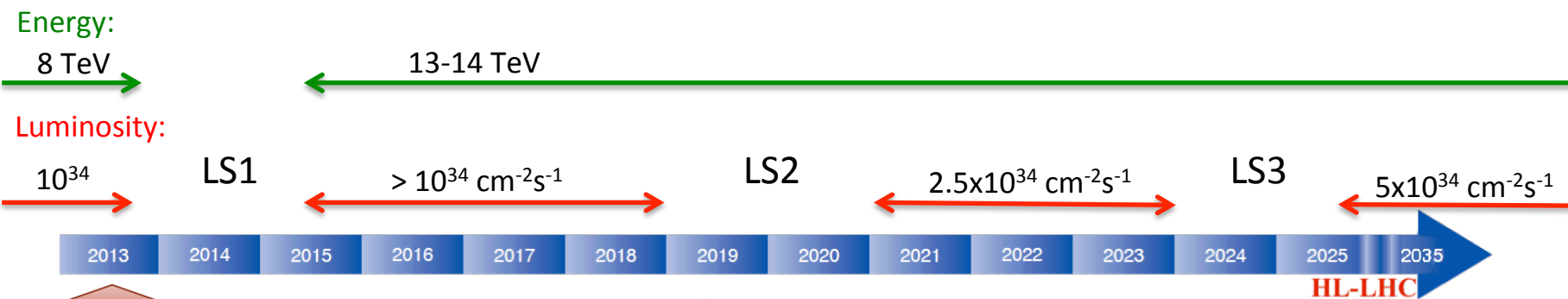# A novel monolithic HV-CMOS pixel detector prototype for the ATLAS upgrade

Stefano Terzo, Emanuele Cavallaro, Raimon Casanova, Fabian Förster, Sebastian Grinstein, Jörn Lange, Carles Puigdengoles

IFAE Pizza Seminar
19th July 2017

Outline

- Introduction
  - The way to the High Luminosity (HL)-LHC
  - The new Inner Tracker (ITk) of ATLAS at HL-LHC
  - A monolithic CMOS silicon sensor for the ITk

- The H35 demonstrator HV-CMOS chip
  - The readout system developed at IFAE
  - The very first beam test measurements of the monolithic matrices

- Conclusions and outlook

Stefano Terzo (IFAE, Barcelona) – Pizza Seminar 19/07/2017

The way to High Luminosity

Energy:

8 TeV

13-14 TeV

Luminosity:

10^{34}

LS1

$> 10^{34}$ cm^{-2}s^{-1}

LS2

2.5×10^{34} cm^{-2}s^{-1}

LS3

5×10^{34} cm^{-2}s^{-1}

2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2035

HL-LHC

Run-I was a success:
- Higgs discovery!!
- Quark-gluon plasma
- Constrains on SUSY
- …

30 fb^{-1}

… but after 2023:
- Marginal statistical gain in running the accelerator
- Need a considerable luminosity increase (collisions per time)

>3000 fb^{-1}

**Run-II + Run-III will bring significant improves:**
- Measure the Standard Model scalar boson properties
- Search for New Physics at higher mass scale

300 fb^{-1}

Stefano Terzo (IFAE, Barcelona) - Pizza Seminar, 19/07/2017

The way to High Luminosity

Energy:

8 TeV → 13-14 TeV

Luminosity:

10^{34} LS1 $> 10^{34}$ cm^{-2}s^{-1} LS2 2.5×10^{34} cm^{-2}s^{-1} LS3 5×10^{34} cm^{-2}s^{-1}

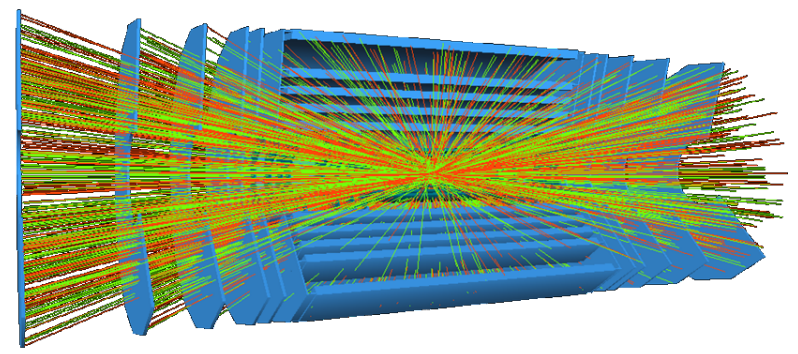2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2035
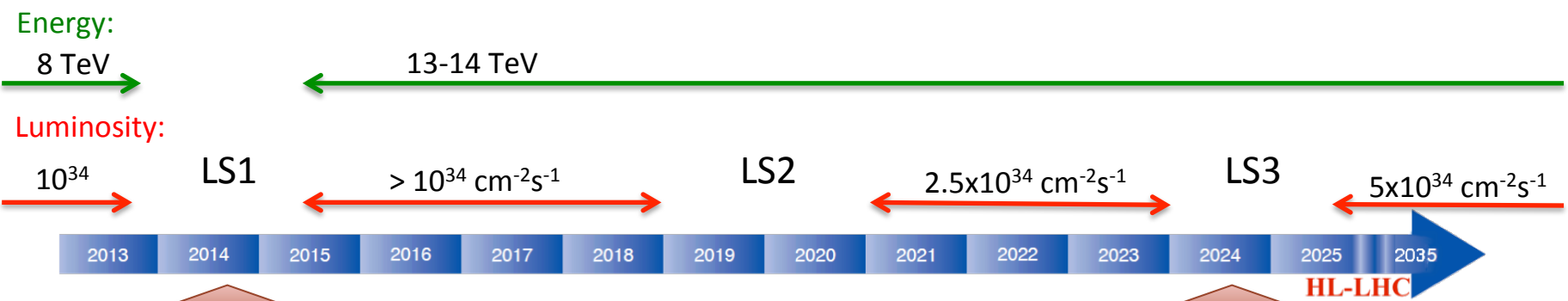
HL-LHC

Insertable B-Layer (IBL): forth pixel layer at 3.2 cm from the beam line

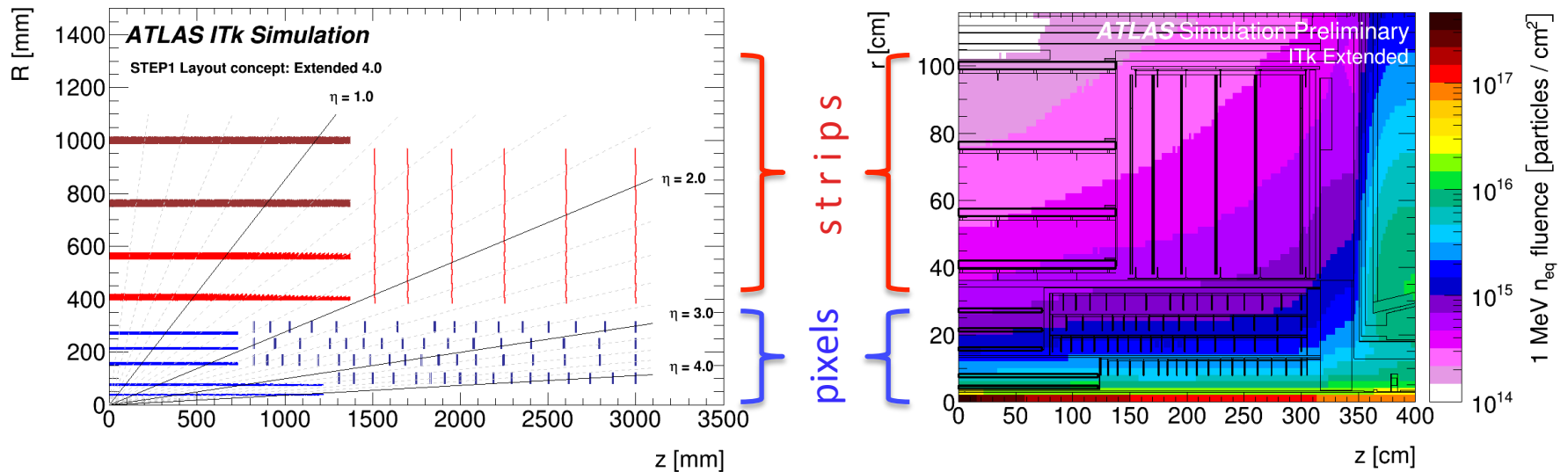**"Phase II":** full inner detector replacement (5 pixel layers)
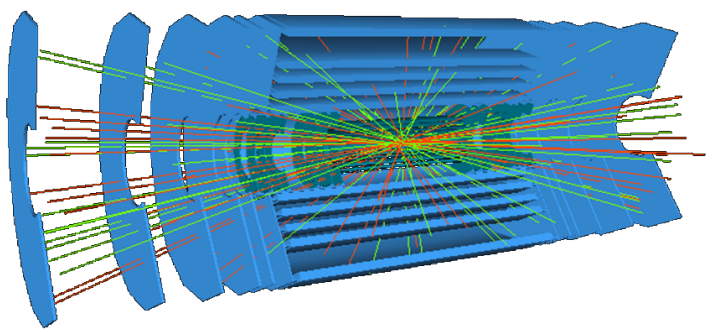
- LHC:
  - 19 Pile-up events

- HL-LHC
  - 140-200 Pile-up events
    → High particle multiplicity
    → Critical radiation damage

4

The ITk upgrade for HL-LHC

Replace the whole ATLAS Inner Detector with a new full-silicon Inner Tracker (ITk)

- New layout with 5 pixel barrel layers & large η coverage

- Sensor technologies under investigation:
  - Outer pixel layers (large area to cover)
    - HR/HV-CMOS pixel detectors
    - n-in-p planar silicon sensors (150 μm thick)
  - Inner pixel layers
    - Thin n-in-p planar silicon sensors (100 μm thick)
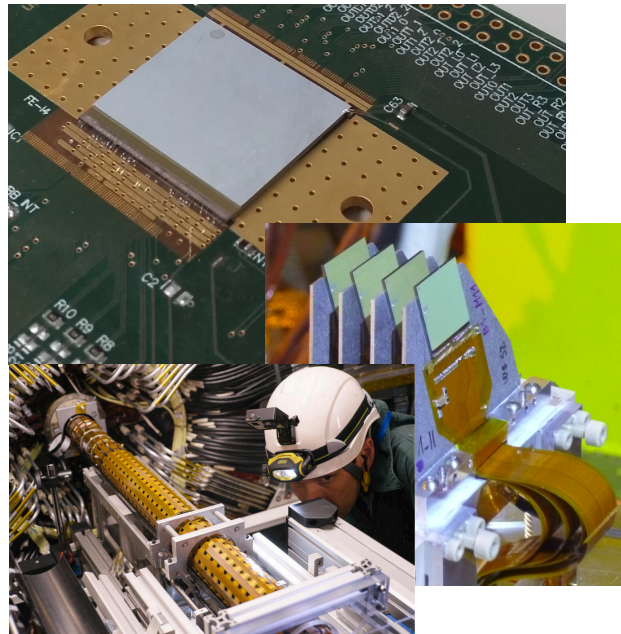   - 3D silicon sensors (baseline for the innermost layer)

Radiation fluence
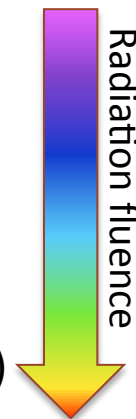
From 1e15 n_{eq}cm^{-2}…
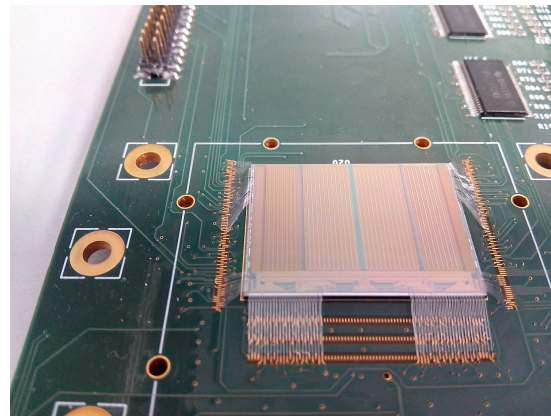
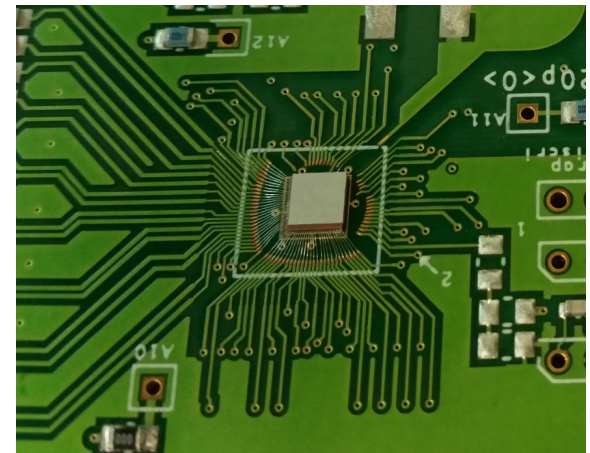…up to 1.7e16 n_{eq}cm^{-2}

The IFAE pixel group activities

Hybrid

3D PIXELS

Already in **IBL** and **AFP**!!

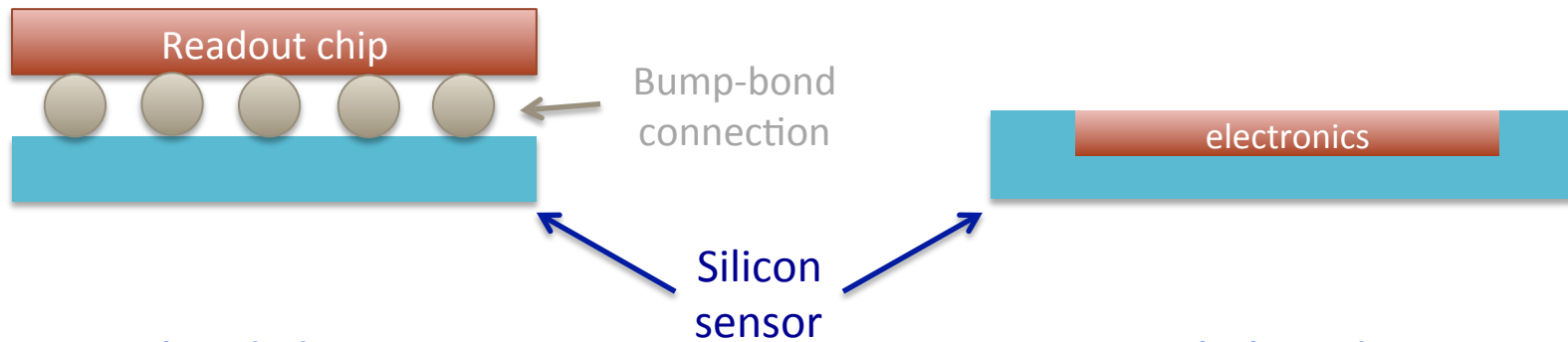**CMOS monolithic pixel detectors**

LGAD detectors for precise timing

Hybrid vs. Monolithic

Readout chip

Bump-bond connection

electronics

Silicon sensor

Hybrid detector

- Sensor + chip

PRO:
- Sensor and chip can be optimized separately
  - ➜ radiation hardness
  - ➜ high rate capability (MHz/mm²)
- Complex signal processing already in the pixel cell

CON:
- Relatively large material budget
  - ➜ multiple scattering
- Complex production and assembly
 - ➜ expensive‼

Monolithic detector

- All in one piece

PRO:
- Commercial technology
- No interconnection costs
  - ➜ cost effective‼
- Low material budget
  - ➜ low multiple scattering

CON:
- Functionalities limited by the size of pixel and dead area at the periphery
- Signal obtained by diffusion
  - ➜ slow‼
  - ➜ not radiation hard‼

Hybrid vs Monolithic

Readout chip

Bump-bond connection

electronics

Silicon sensor

Monolithic detector

Hybrid detector
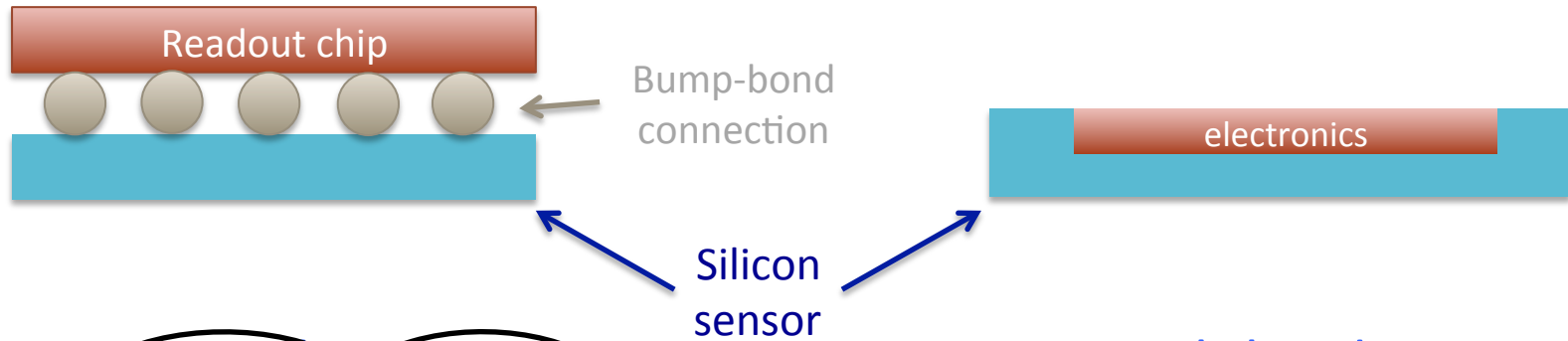
How to overcome these limitations in the present CMOS technology?

- Smaller and more radiation hard electronics
  - CMOS process can go down to 150 nm and less
- Depleted Monolithic Active Pixels Sensors (DMAPS)
  - High voltage
  - High resistivity $\left.\right\}$ $d \propto \sqrt{\rho V}$

in the

CON:

- Relatively large material
  → multiple scattering
- Complex production and assembly
  → expensive!!

...nalities limited by the size of pixel and dead area at the periphery
Signal obtained by diffusion
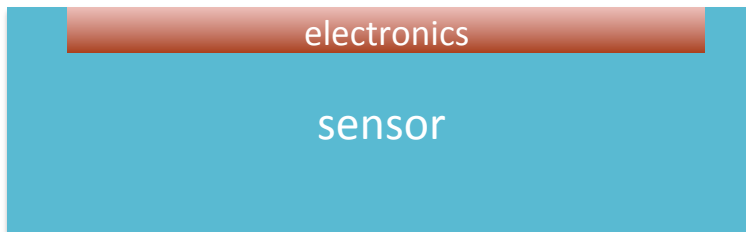 → slow!!
  → not radiation hard!!

7

Monolithic

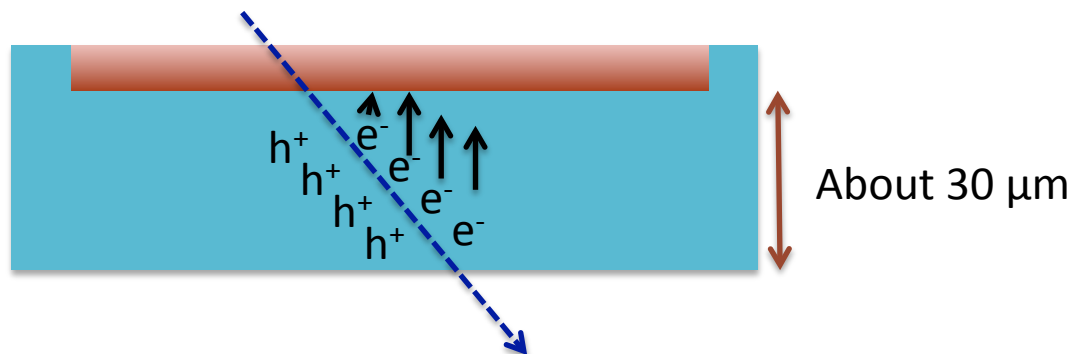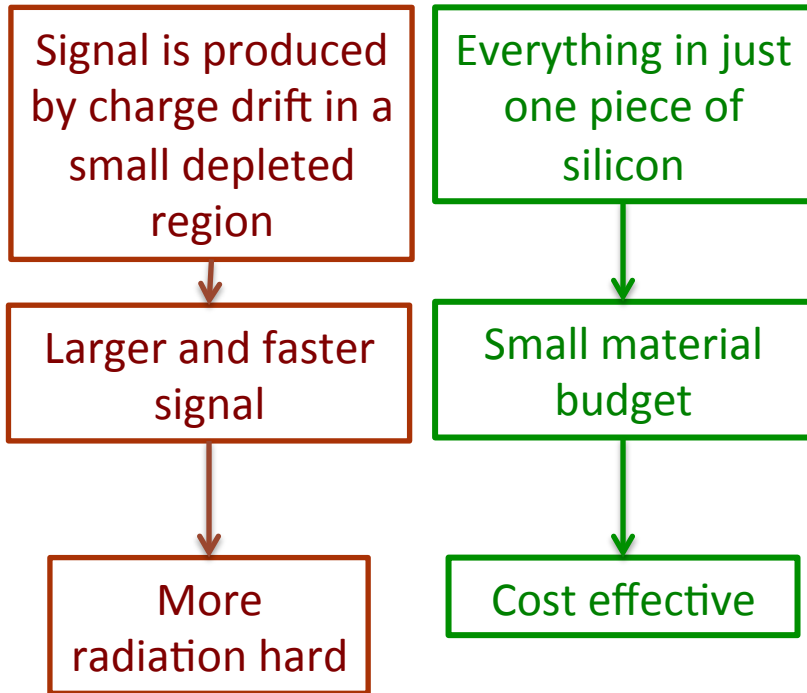Everything in just one piece of silicon
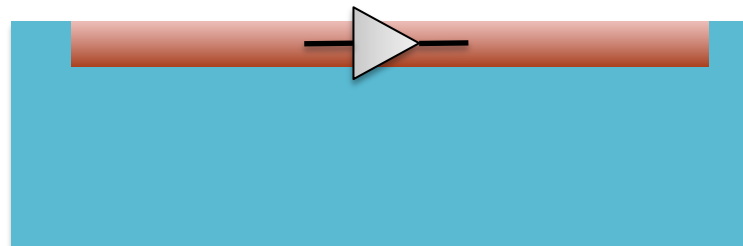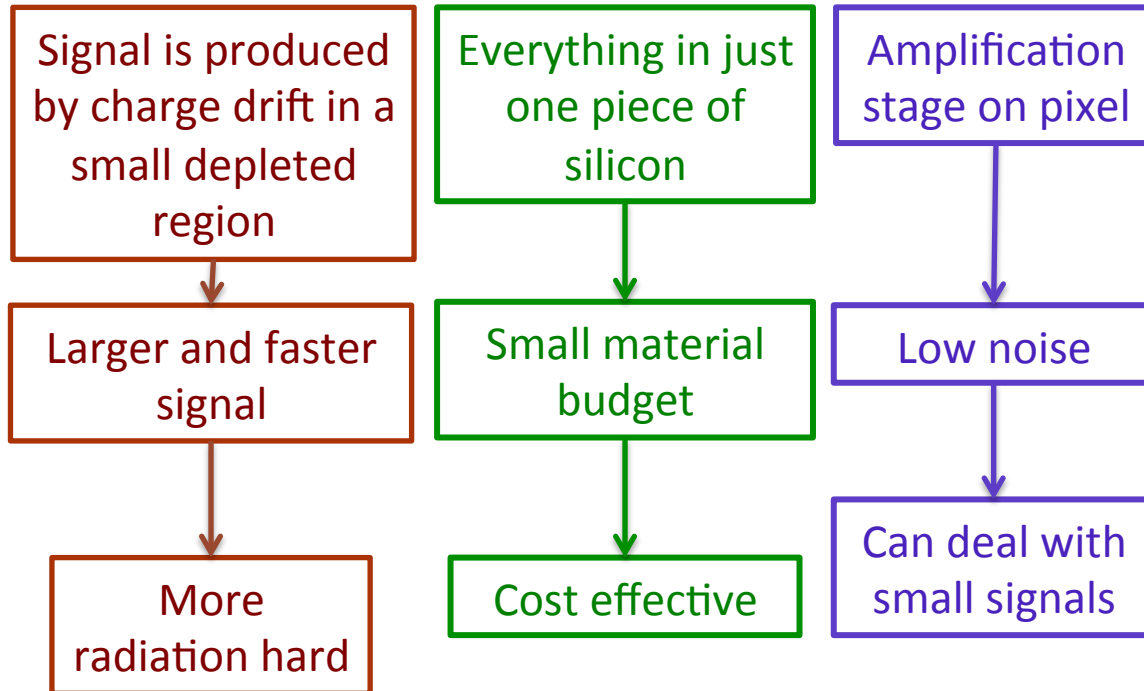
↓

Small material budget

↓

Cost effective

electronics

sensor

DMAPS

Depleted Monolithic

Signal is produced by charge drift in a small depleted region	Everything in just one piece of silicon
↓	↓
Larger and faster signal	Small material budget
↓	↓
More radiation hard	Cost effective

About 30 μm

DMAPS

Depleted Monolithic Active

Signal is produced by charge drift in a small depleted region	Everything in just one piece of silicon	Amplification stage on pixel
↓	↓	↓
Larger and faster signal	Small material budget	Low noise
↓	↓	↓
More radiation hard	Cost effective	Can deal with small signals

DMAPS

Depleted Monolithic Active Pixel Sensors
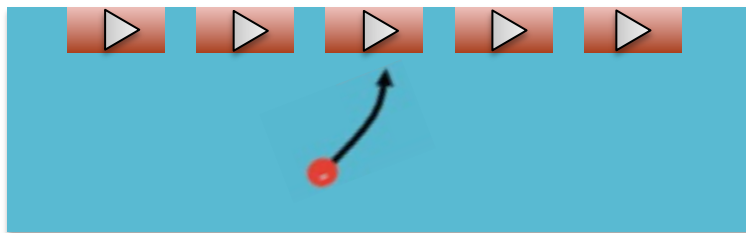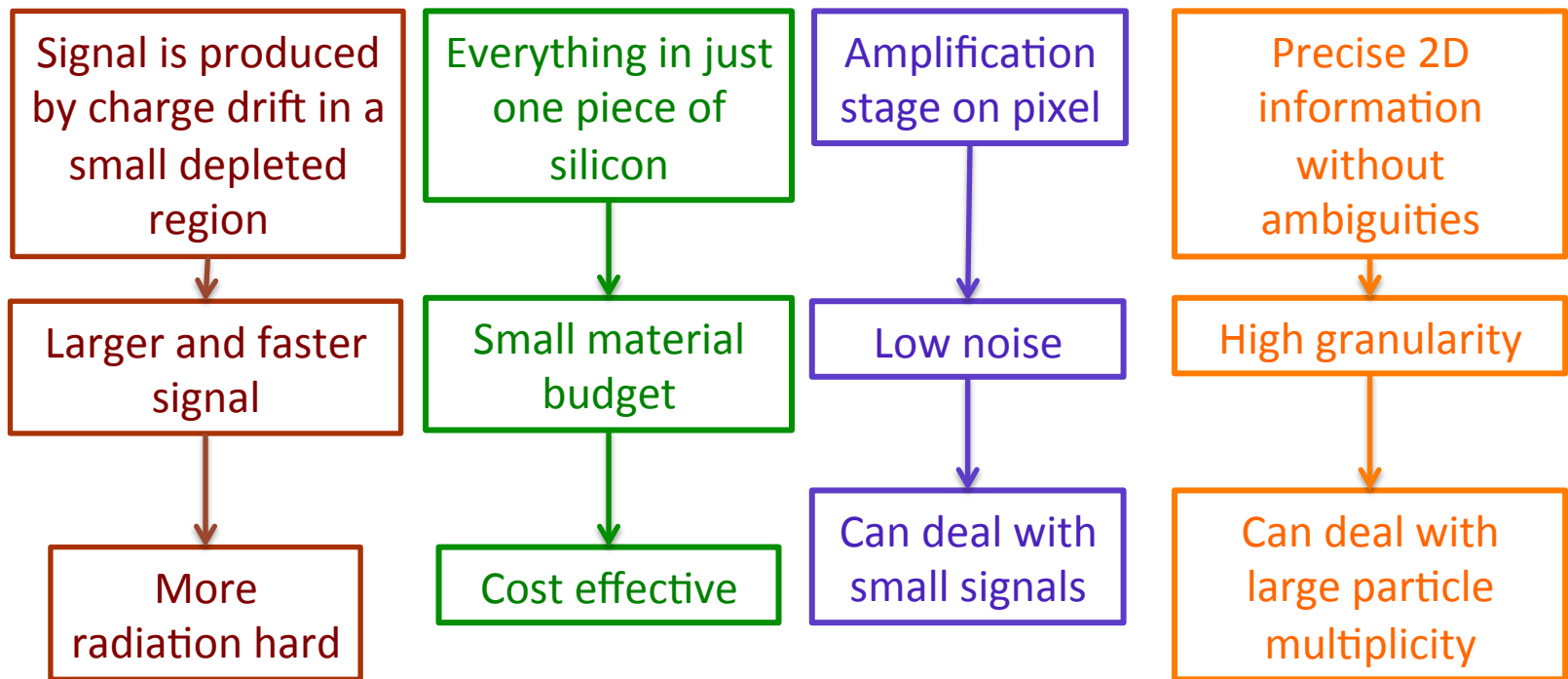
Signal is produced by charge drift in a small depleted region	Everything in just one piece of silicon	Amplification stage on pixel	Precise 2D information without ambiguities
↓	↓	↓	↓
Larger and faster signal	Small material budget	Low noise	High granularity
↓	↓	↓	↓
More radiation hard	Cost effective	Can deal with small signals	Can deal with large particle multiplicity

Stefano Terzo (IFAE, Barcelona) - Pizza Seminar, 19/07/2017

The H35 Demonstrator

AMS 350 nm High Voltage CMOS w. different ρ: 20–80–200–1000 Ωcm
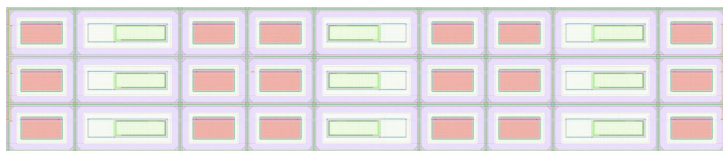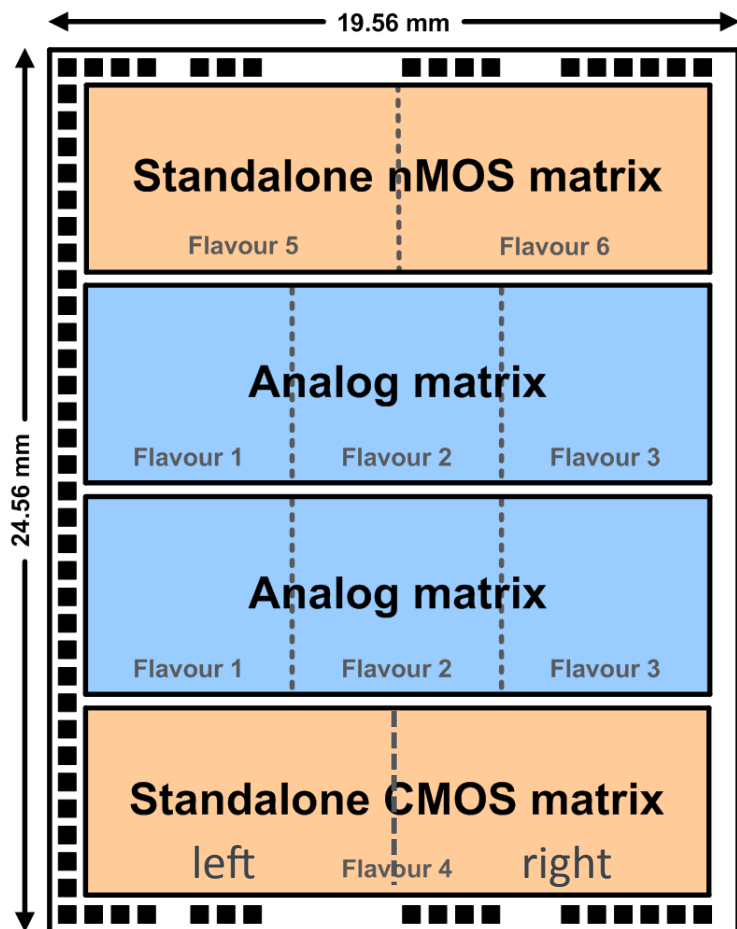
- **Monolithic nMOS matrix**:
  - Digital pixels with in-pixel nMOS comparator
  - Two flavors: with and without Time Walk compensation

- **Analog matrices (2 arrays):**
  - To be used as hybrid modules with ATLAS chips

- **Monolithic CMOS matrix**:
  - Analog pixels with off-pixel CMOS comparator

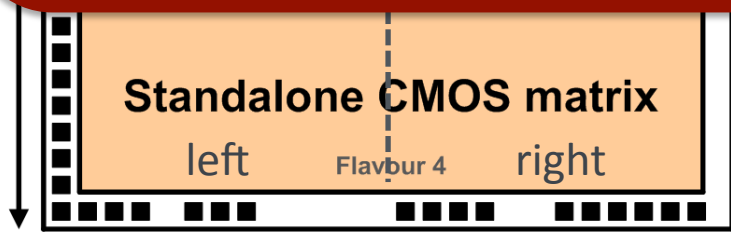Designed by KIT, IFAE and Univ. of Liverpool

+ test structures without electronics

The H35 Demonstrator

AMS 350 nm High Voltage CMOS w. different ρ: 20–80–200–1000 Ωcm
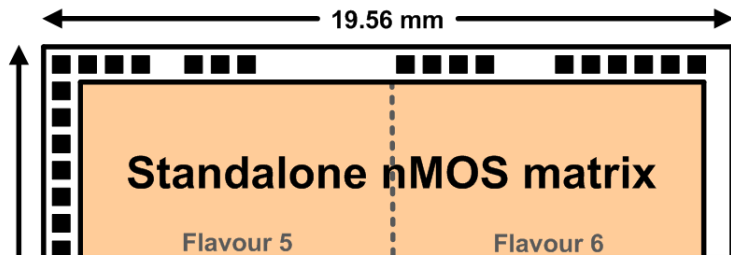
- **Monolithic nMOS matrix**:
  - Digital pixels with in-pixel nMOS comparator

Large collaboration

  - Analog pixels with off-pixel CMOS comparator

Designed by KIT, IFAE and Univ. of Liverpool

+ test structures without electronics

The H35 pixel structure
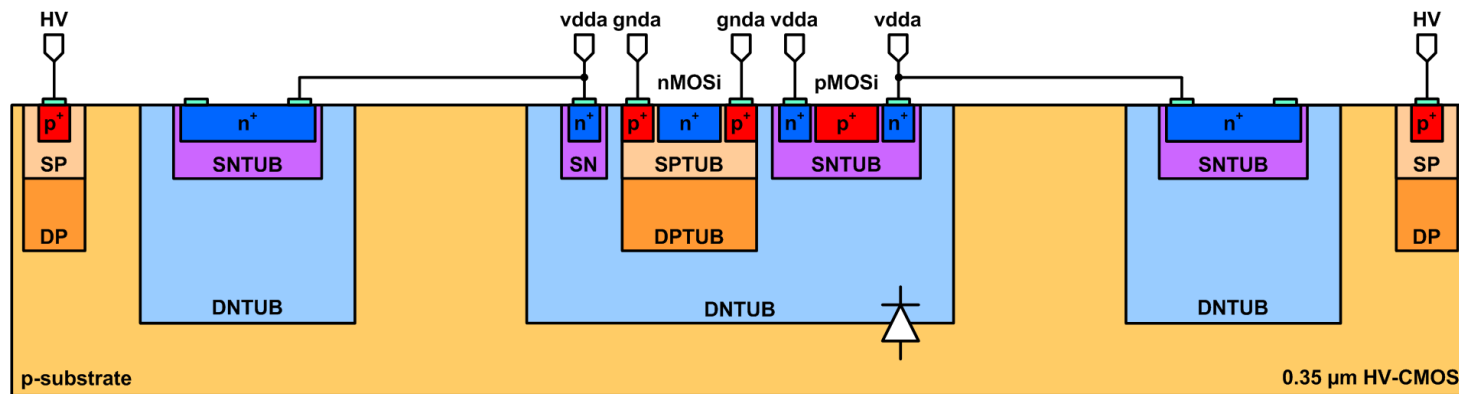
- Pixel size is the same as the present ATLAS sensor in IBL:
  - 50x250 μm^2
  - Electronics inside the n-well used as collecting electrode
  - p-substrate + 3 separate deep n-wells* to reduce the capacitance
    - ➔ Less noise, better timing - power consumption
    - ➔ Dimensions depend on the in-pixel functionalities

- Bias voltage applied from the top
  - Single side processing
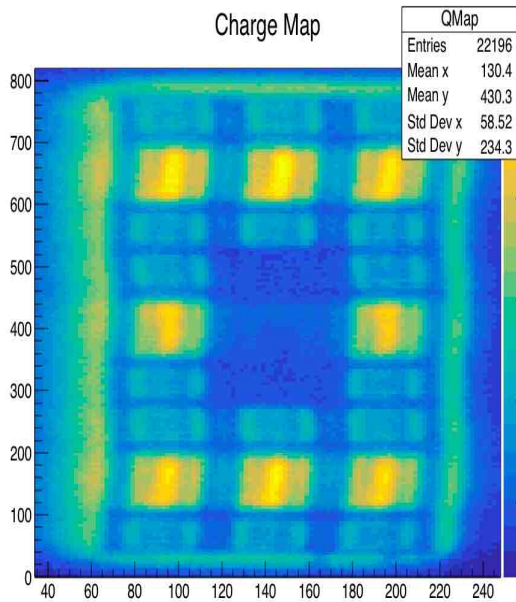   - ➔ Cheaper
    - ➔ Non-uniform electric field

*all matrices but monolithic nMOS

Studies with laser

- Investigation of passive test structures with infra-red laser
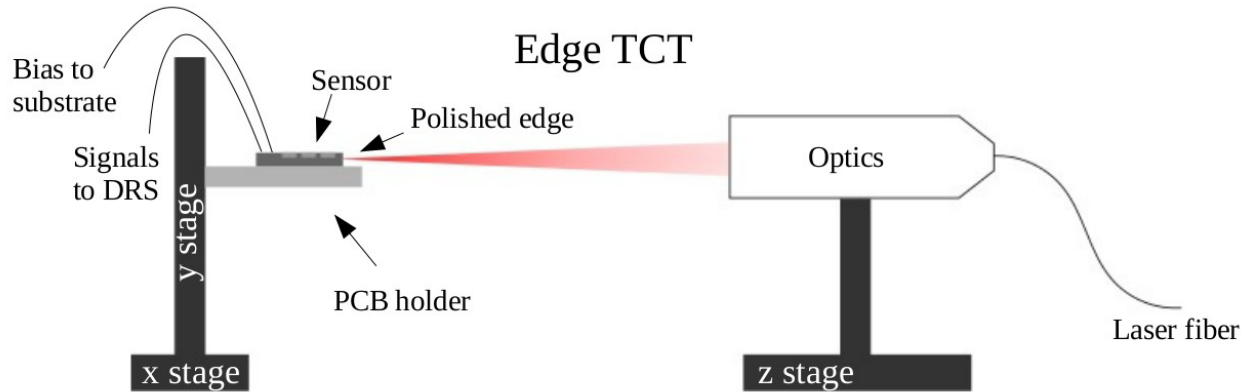
Investigation of the charge collection properties of the silicon sensor (without electronics)
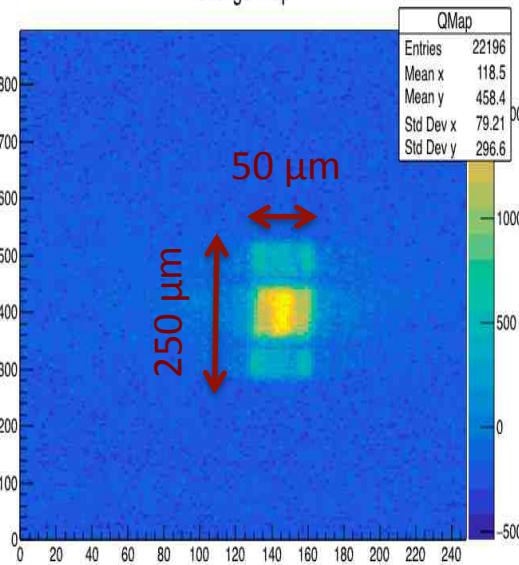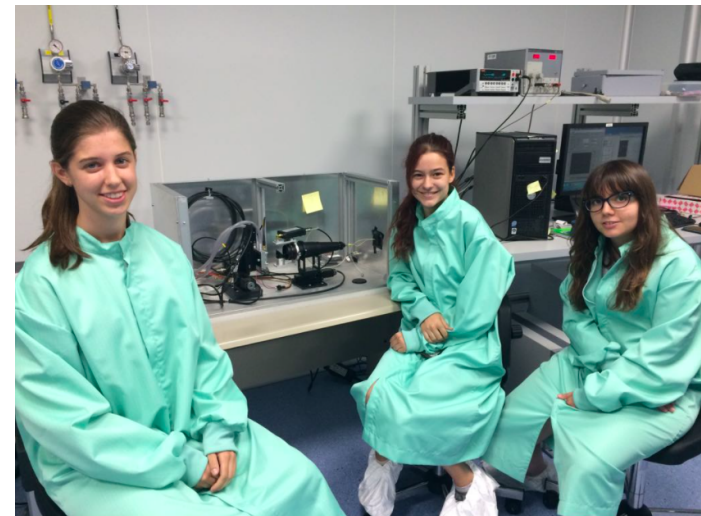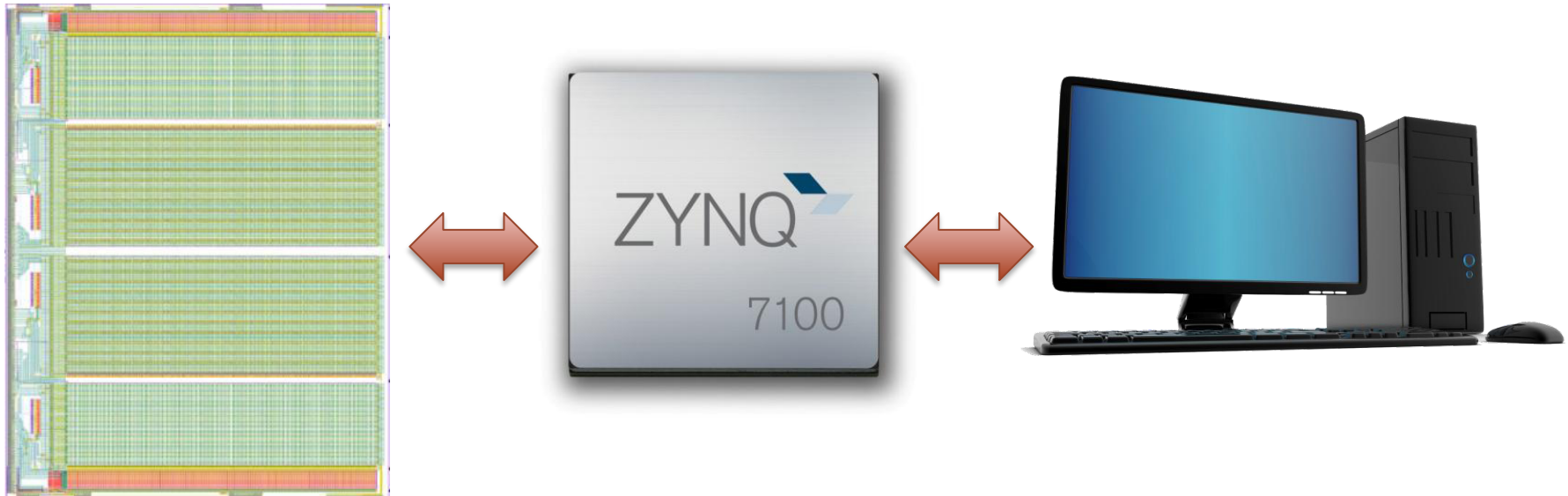

A team of young researchers working on it!!

The readout system

Communication with configuration register

H35Demo
- Communication protocol not compatible with PC ports

FPGA
- FPGA acts a communications bridge
- Communicate with the H35Demo

Control PC
- Software with Graphical User Interface (GUI)
- Send commands and receive data from the FPGA

People involved

Stefano Terzo (IFAE, Barcelona) - Pizza Seminar, 19/07/2017

Chip design
Ivan Peric (KIT)
Raimon Casanova
Eva Vilella (Liv.)
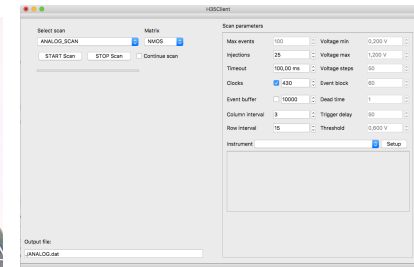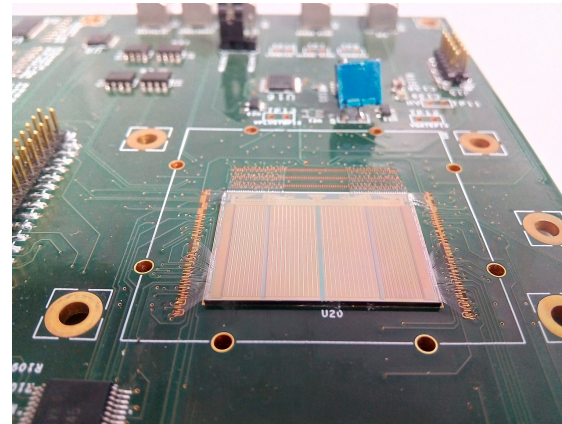
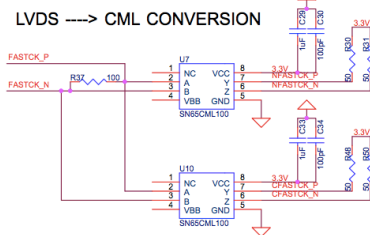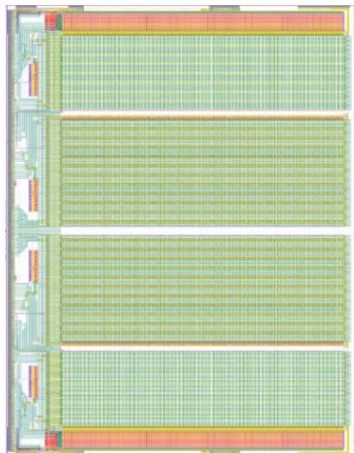**PCB design &
FPGA programming**
Carles Puigdengoles

**Assembly &
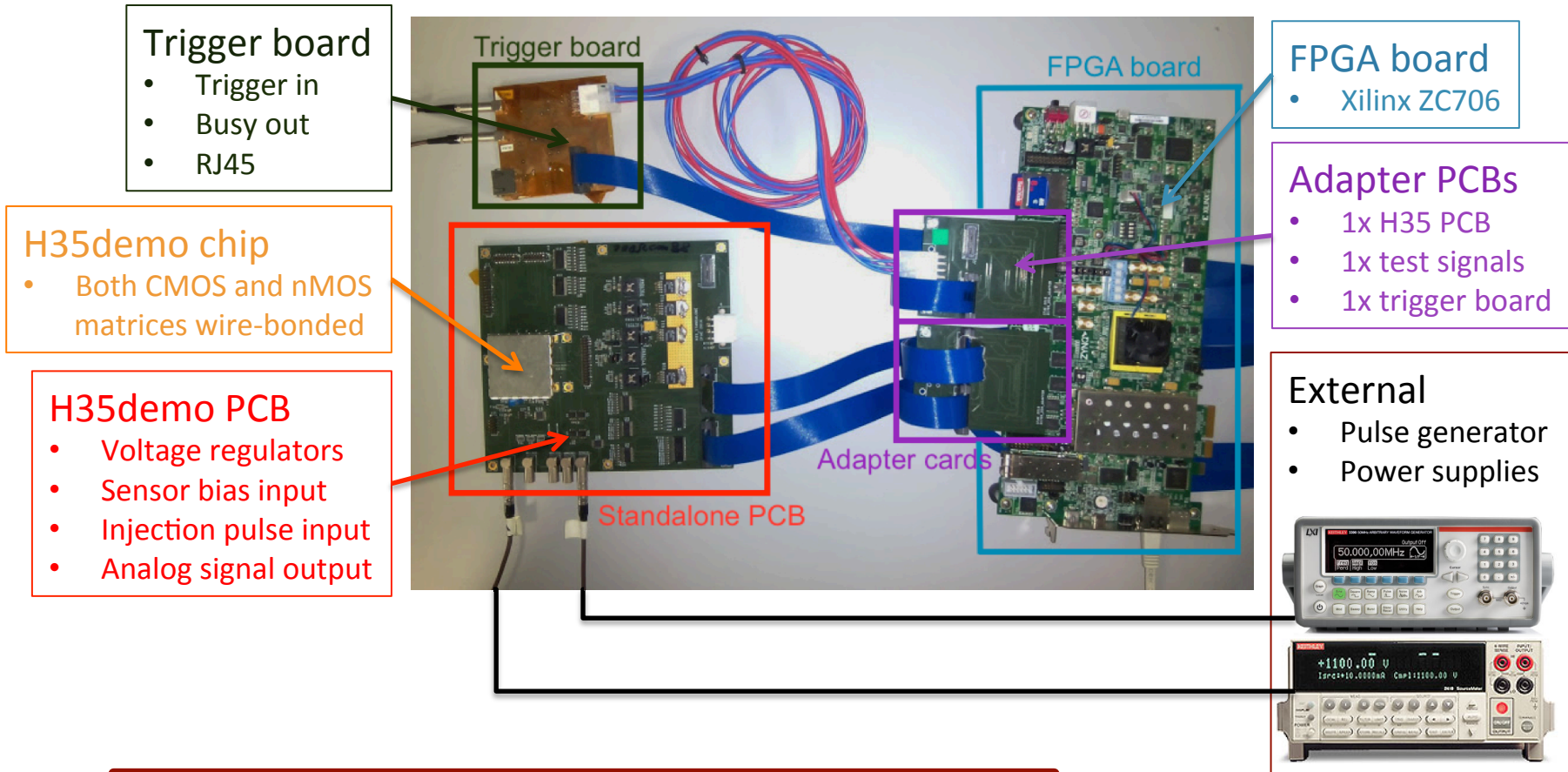Wire-bond**
Jorge Garcia Rodriguez
Eric Peregrina

**Software &
Charcterization**
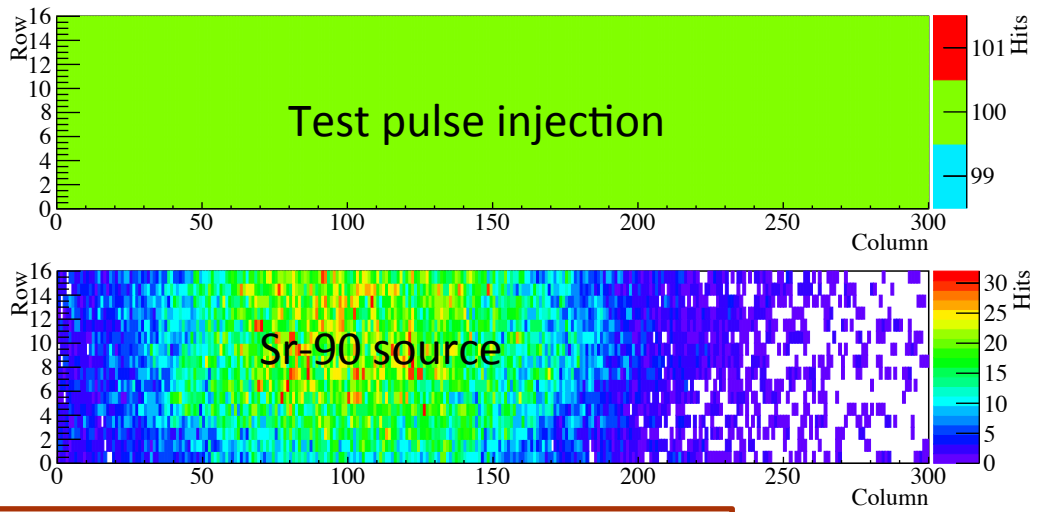Emanuele Cavallaro
Fabian Förster
Stefano Terzo
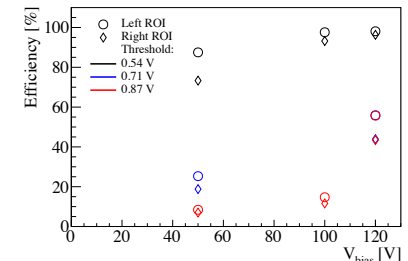
PCBs, firmware and software fully developed at IFAE

13

Monolithic matrix readout at IFAE

Trigger board
- Trigger in
- Busy out
- RJ45

H35demo chip
- Both CMOS and nMOS matrices wire-bonded

H35demo PCB
- Voltage regulators
- Sensor bias input
- Injection pulse input
- Analog signal output

FPGA board
- Xilinx ZC706

Adapter PCBs
- 1x H35 PCB
- 1x test signals
- 1x trigger board

External
- Pulse generator
- Power supplies

Same base setup also used for
Medipix3 (RIS3CAT) and
HV-CMOS LF (Photon counting + ATLAS)

Stefano Terzo (IFAE, Barcelona) - Pizza Seminar, 19/07/2017

Operations and tests

Test pulse injection

Sr-90 source
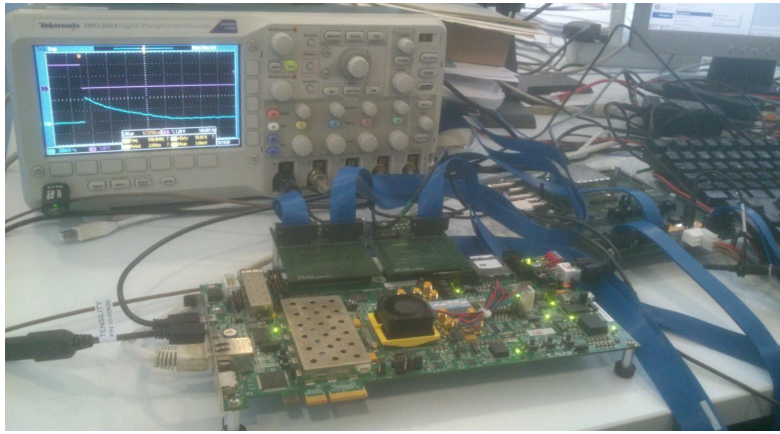
Test of the functionalities and tuning of the pixel thresholds

SCurve Pixel 23 6

One pixel

Noise

threshold

Injected pulse amplitude [V]

Full Matrix - 0.87 V

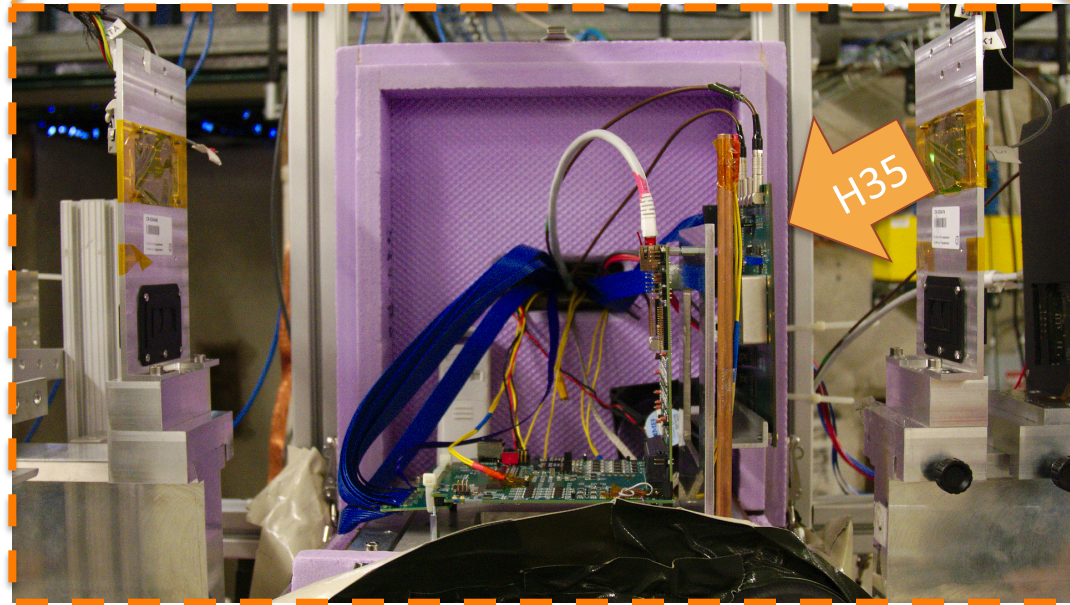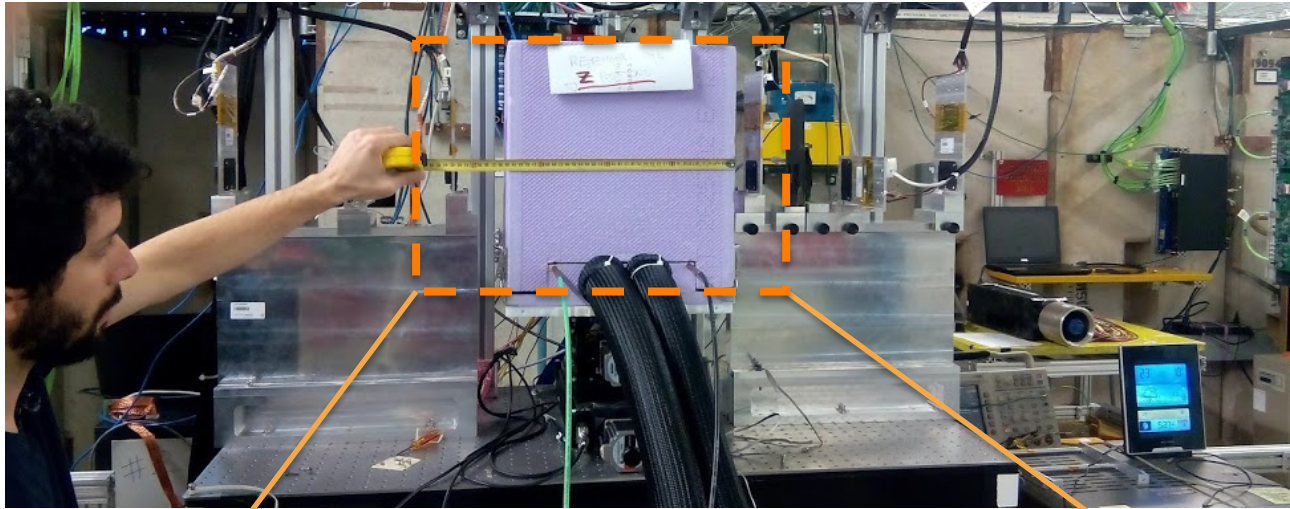Left Matrix - 0.84 V

Right Matrix - 0.89 V

Threshold [V]
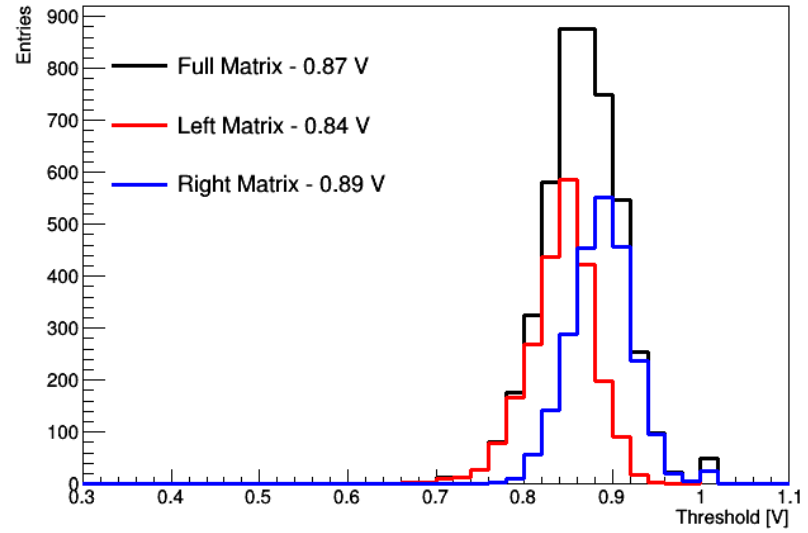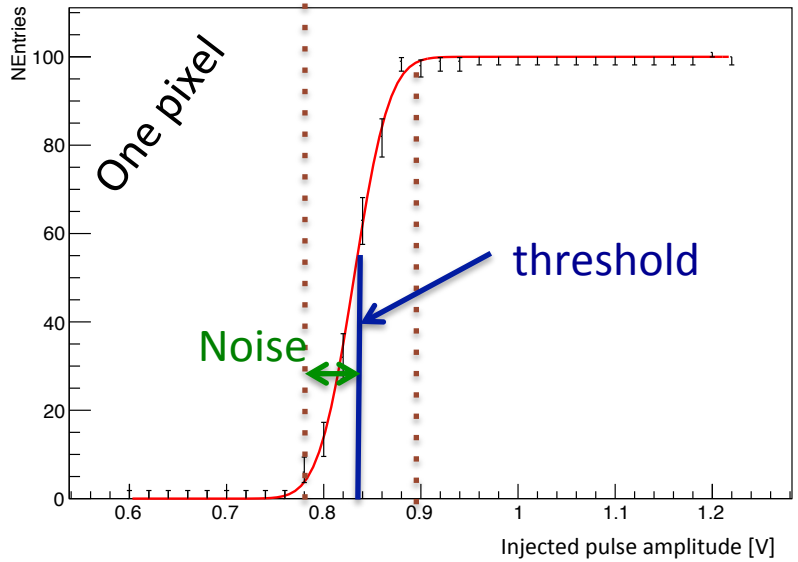
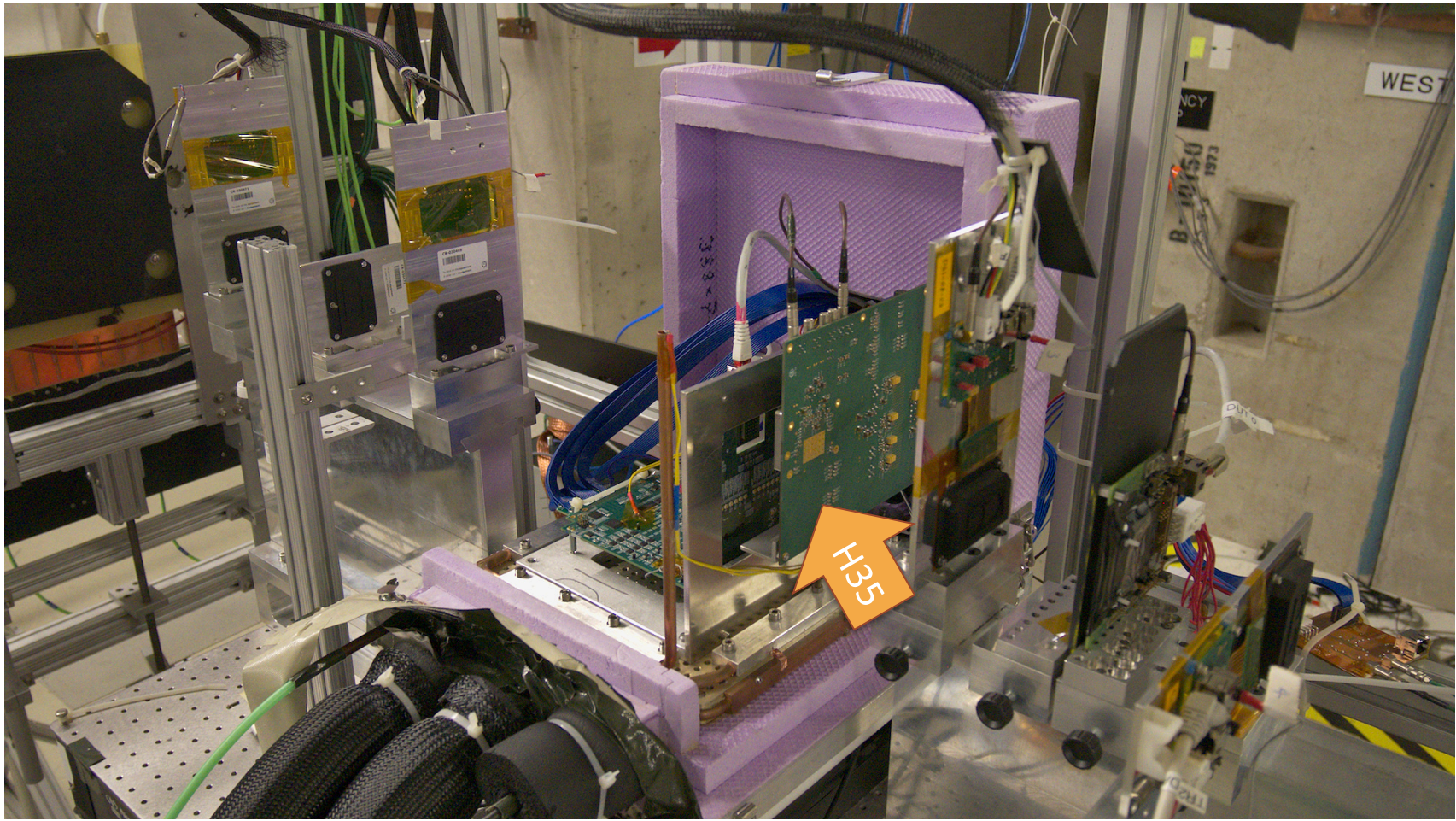# Test beam setup I

UinGe FE-I4 Telescope
+
IFAE readout system
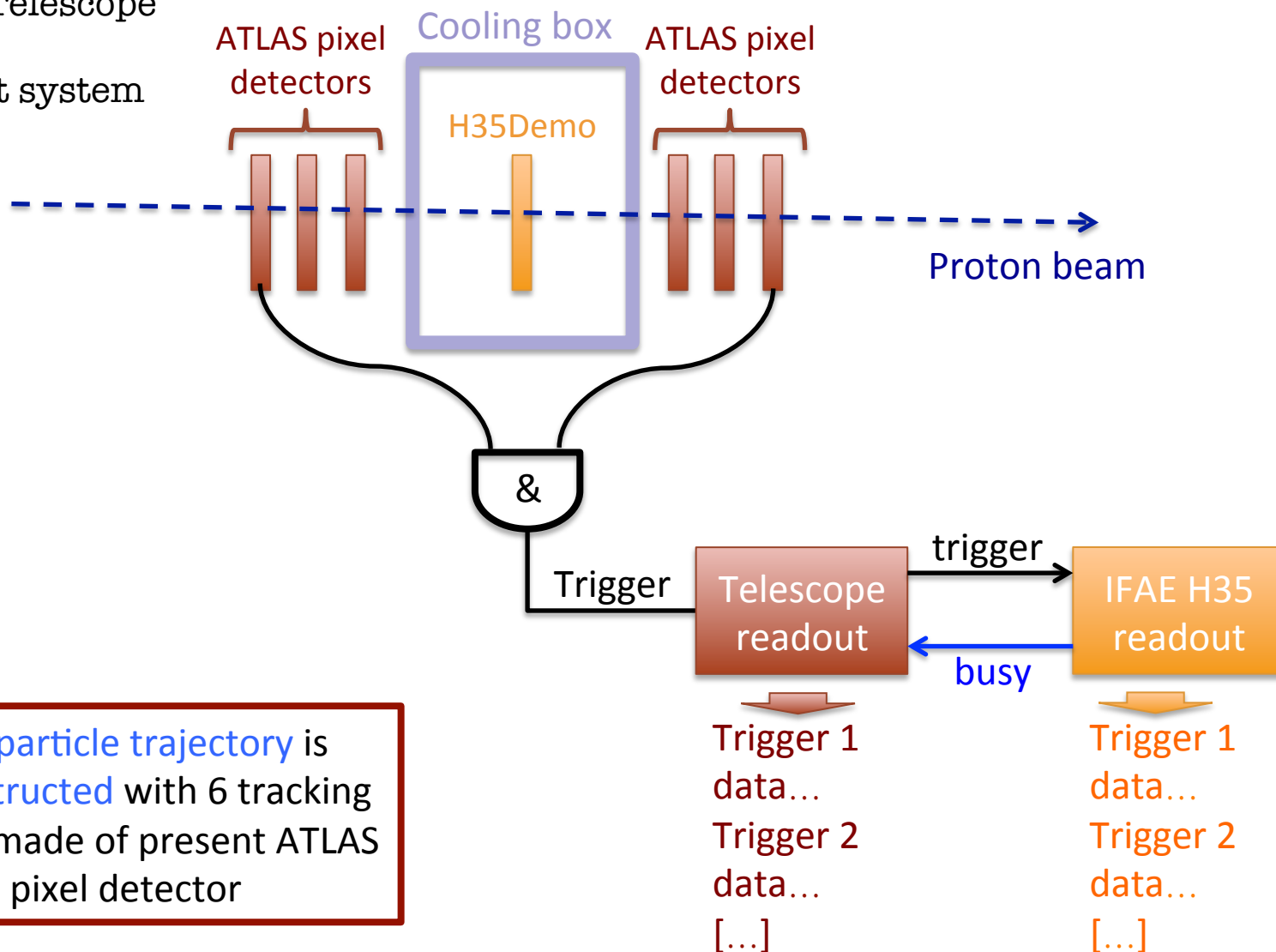
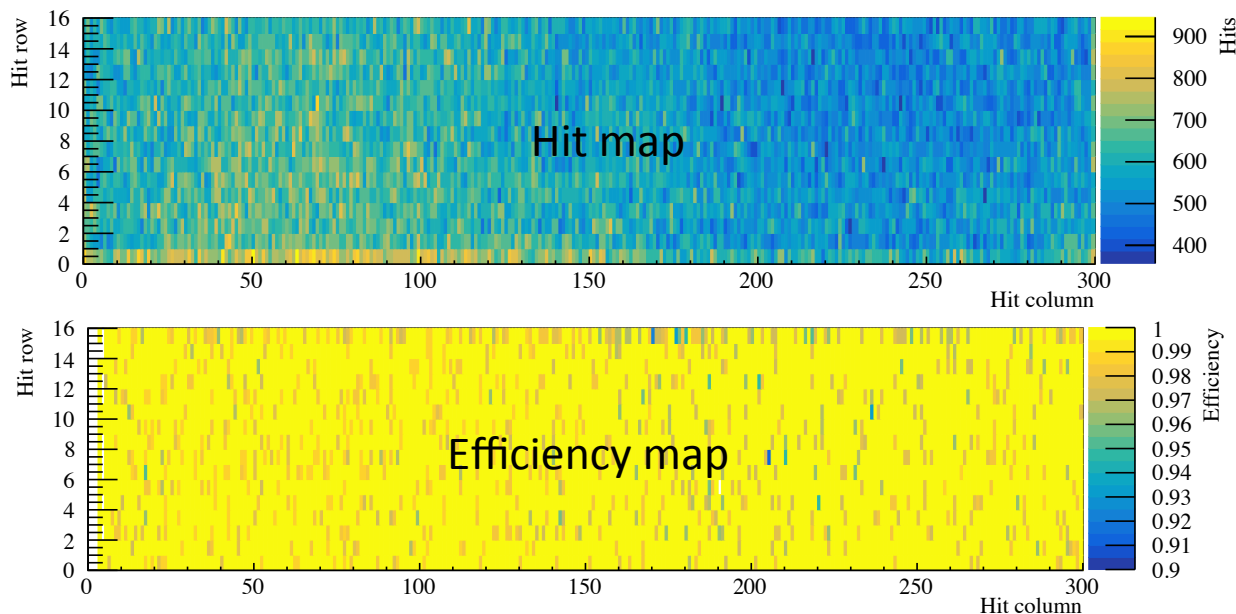The particle trajectory is reconstructed with 6 tracking planes made of present ATLAS pixel detector

Test beam setup II
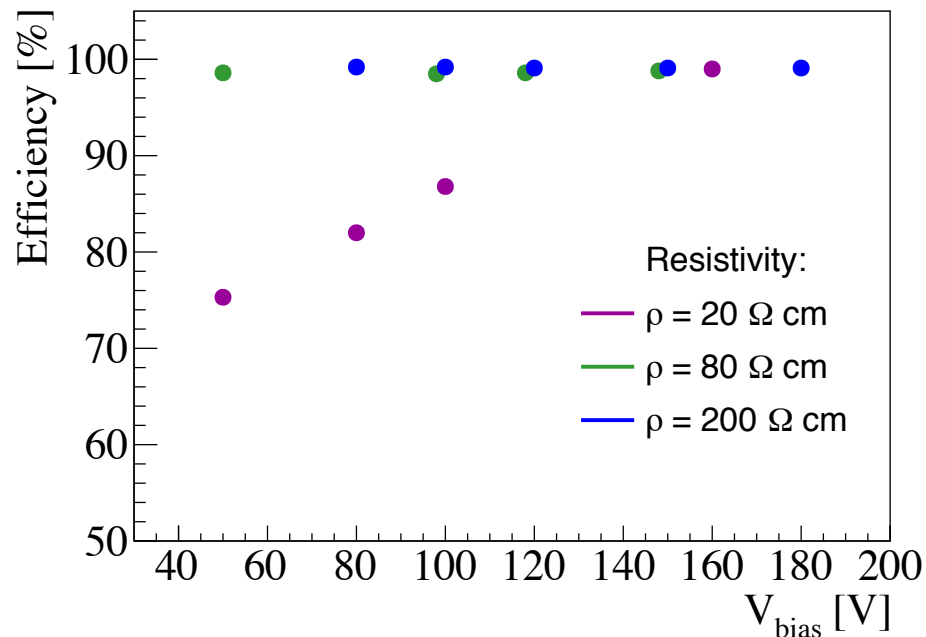
Test beam setup III

H35

Hit efficiency results

Efficiency
=
# of hits in the H35
———————————————
# of tracks reconstructed

- ## Before irradiation
  - Uniform efficiency
  - For $\rho \geq 80$ Ωcm
    - Efficiency > 99%
    - for $V_{bias} \geq 50$ V
  - For $\rho = 20$ Ωcm
    - Efficiency reach 99% at 160 V
    - Depletion depth too low up to 100 V

Resistivity:
— $\rho = 20$ Ω cm
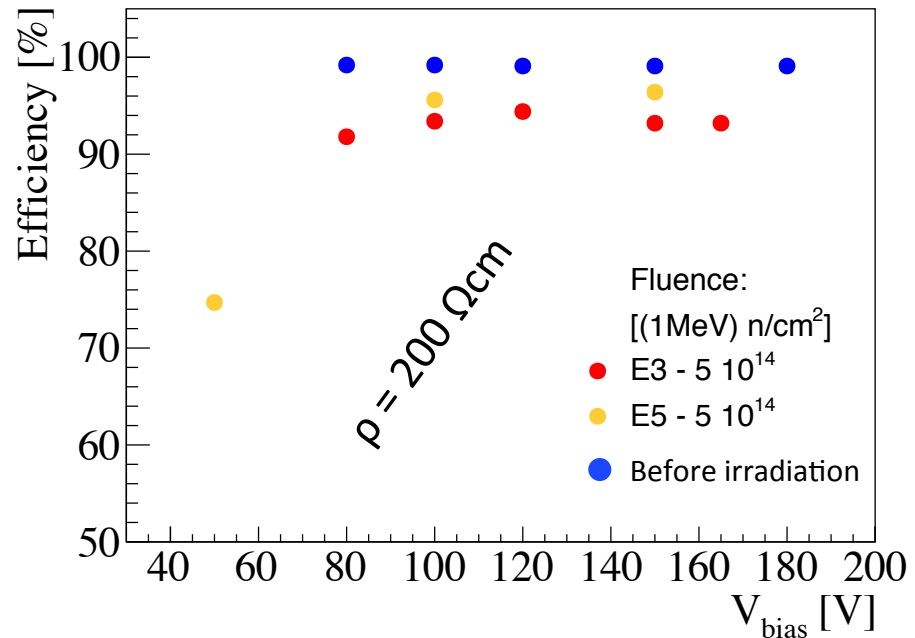— $\rho = 80$ Ω cm
— $\rho = 200$ Ω cm

19

Irradiated detectors
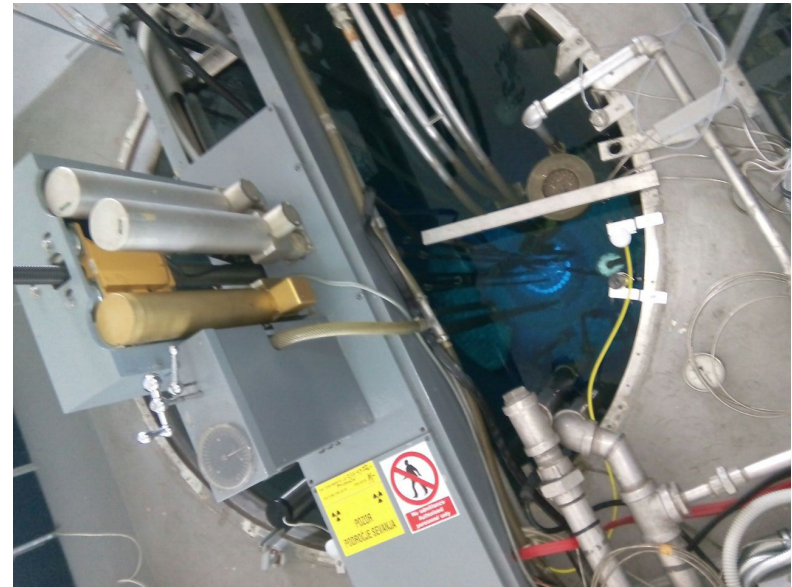
The chip are then irradiated with neutrons in the TRIGA reactor in Ljubljana

After irradiation the functionality of the chip is checked in the laboratory

…and it is again measured at the beam test

- After irradiation to 5e14 $n_{eq}cm^{-2}$
  - For ρ = 200 Ωcm
    - Efficiency > 90%
    - for Vbias ≥ 80 V

Efficiency [%] vs V_{bias} [V]

ρ = 200 Ωcm

Fluence:
[(1MeV) n/cm^2]
- E3 - 5 10^{14}
- E5 - 5 10^{14}
- Before irradiation

Conclusions & outlook

- New readout system developed at IFAE to operate the monolithic part of the H35Demo chip
  - Used at IFAE for CMOS and RIS3CAT, and adopted by University of Bern
  - Base system adaptable to test the future chip generations

- First characterization of monolithic device for ATLAS
  - Full efficiency measured before irradiation at test beam
  - First result of irradiated modules are promising considered the limitations of this first monolithic prototype chip (continuous readout, no masking of noisy pixels, …)

- What's next:
  - Full characterization of the H35Demo prototype after neutron and proton irradiations ongoing (next test beam in September/October)
  - New prototypes with more complex readout system are being designed and produced with the aim of develop a chip which fully meet the ATLAS specification (radiation hardness, timing, power consumption, …)

> It is not clear if ATLAS will adopt Depleted-CMOS for 5th pixel layer,
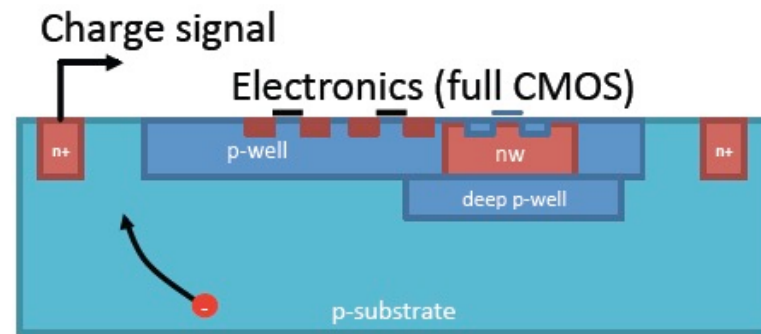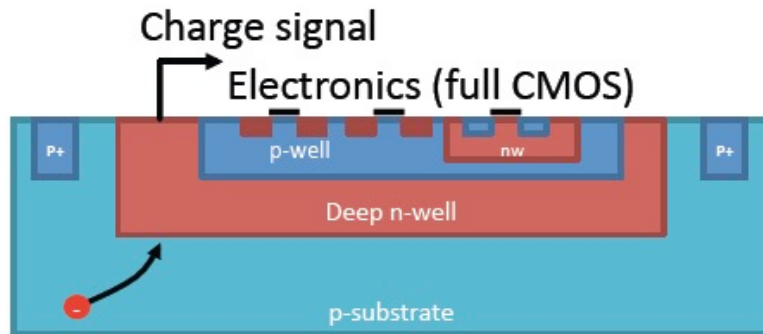> But right now is an option that is being fully investigated

Questions?

Backup slides

HV-CMOS Depleted MAPS

Two different philosophies:

- **Electronics inside the n-well**
  - Large fill factor:
    - PRO:
      - Uniform electric field
      - Short charge drift
        - ➔ Radiation hardness!!
    - CON:
      - Large sensor capacitance (~100 fF)
        - ➔ More noise
        - ➔ Power and speed??

- **Electronics outside the n-well**
  - Small fill factor:
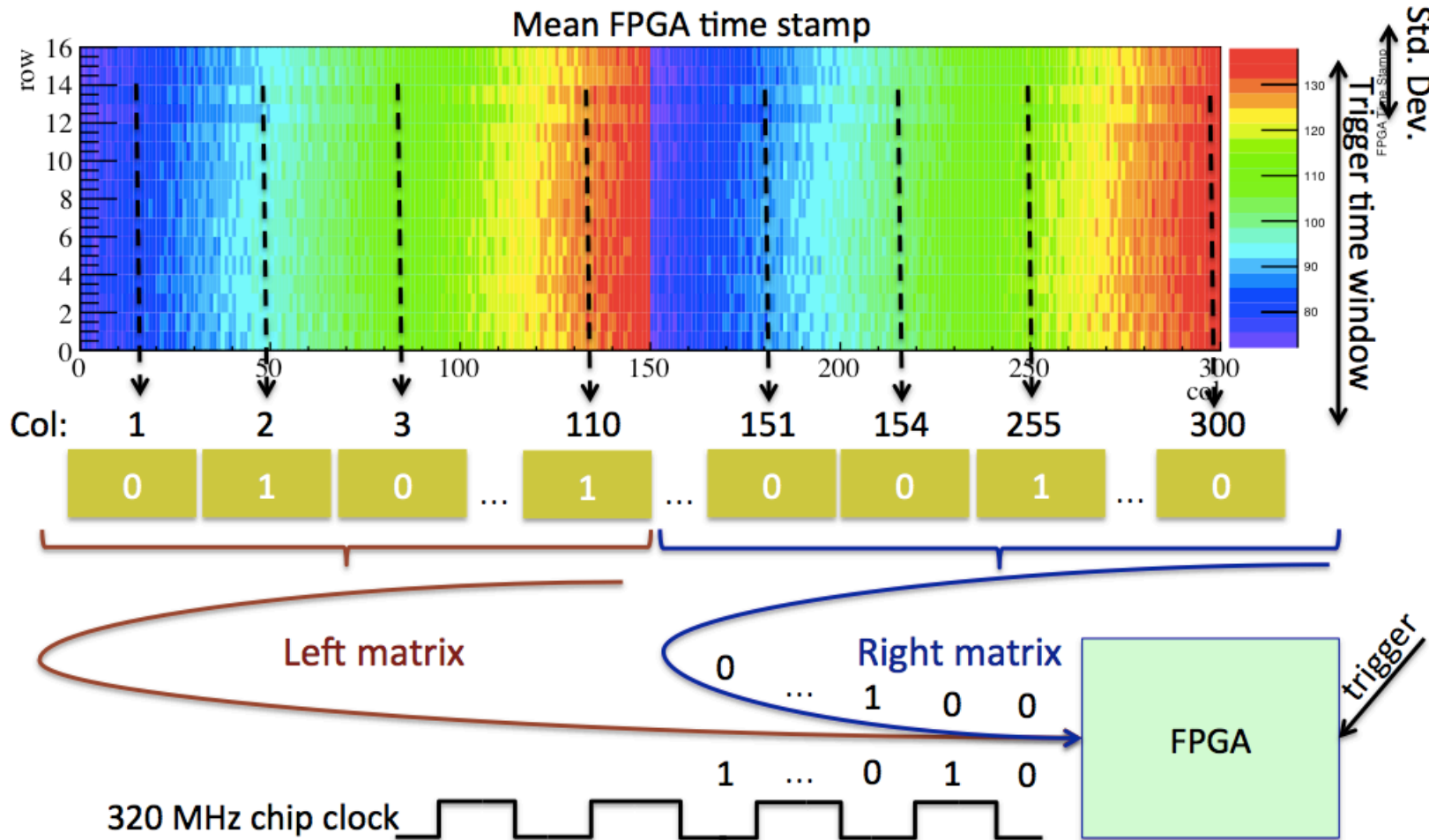   - PRO:
      - Very small capacitance (~5 fF)
        - ➔ Low noise
        - ➔ Low power, high speed!!
    - CON:
      - Low electric field regions
      - Long drift distance
        - ➔ Radiation hardness??
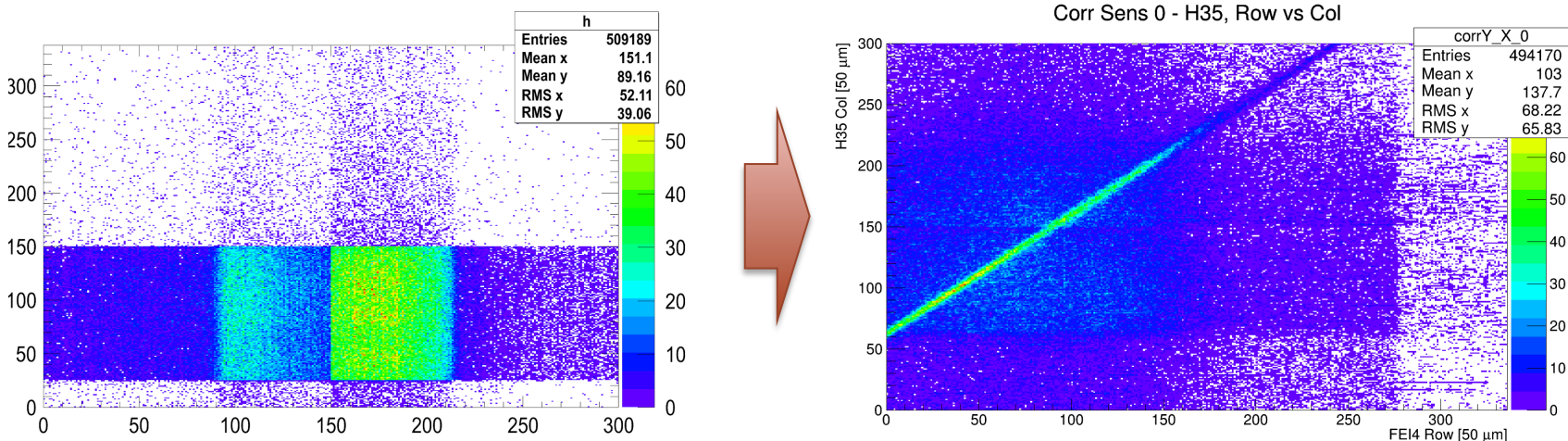
Readout and trigger

Mean FPGA time stamp

- Column drain architecture with priority encoding (same as ATLAS FE-I3 chip)
- Limitations of the H35 demonstrator chip
  - Un-triggered readout ➜ trigger logic implemented in the FPGA
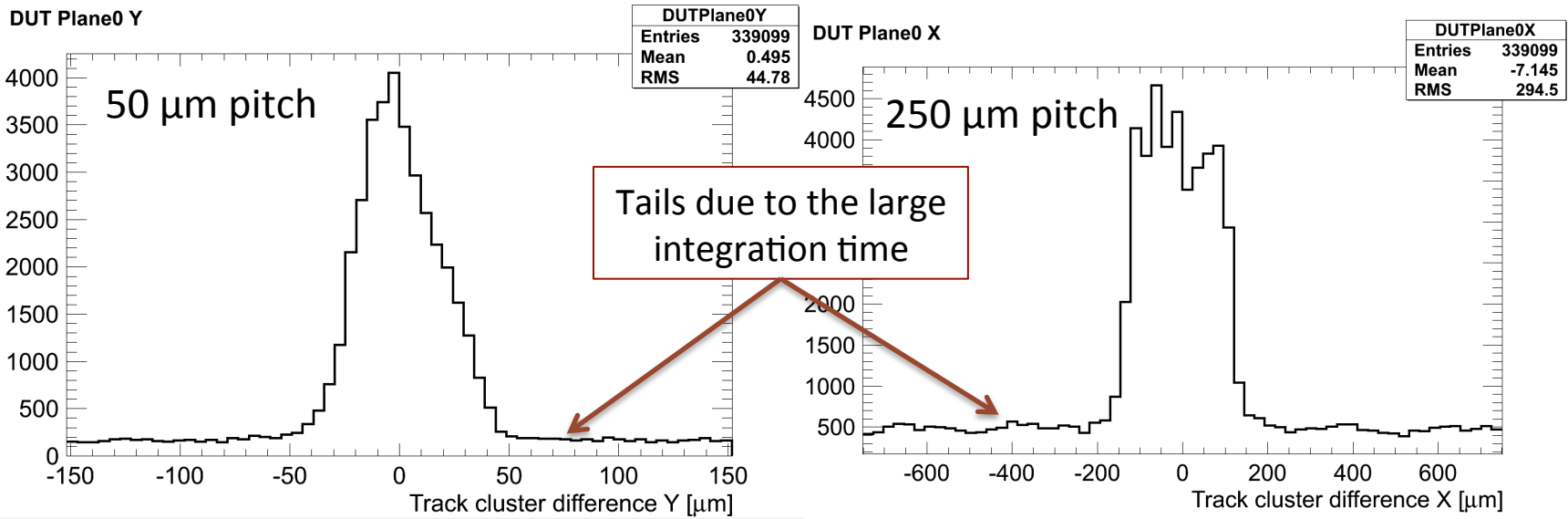 - No zero suppression ➜ also performed at the FPGA level

Long readout time (>1 μs)

Synchronization and alignment

- Correlations between the hits in the H35 CMOS matrix and a telescope plane show the successful synchronization of the data
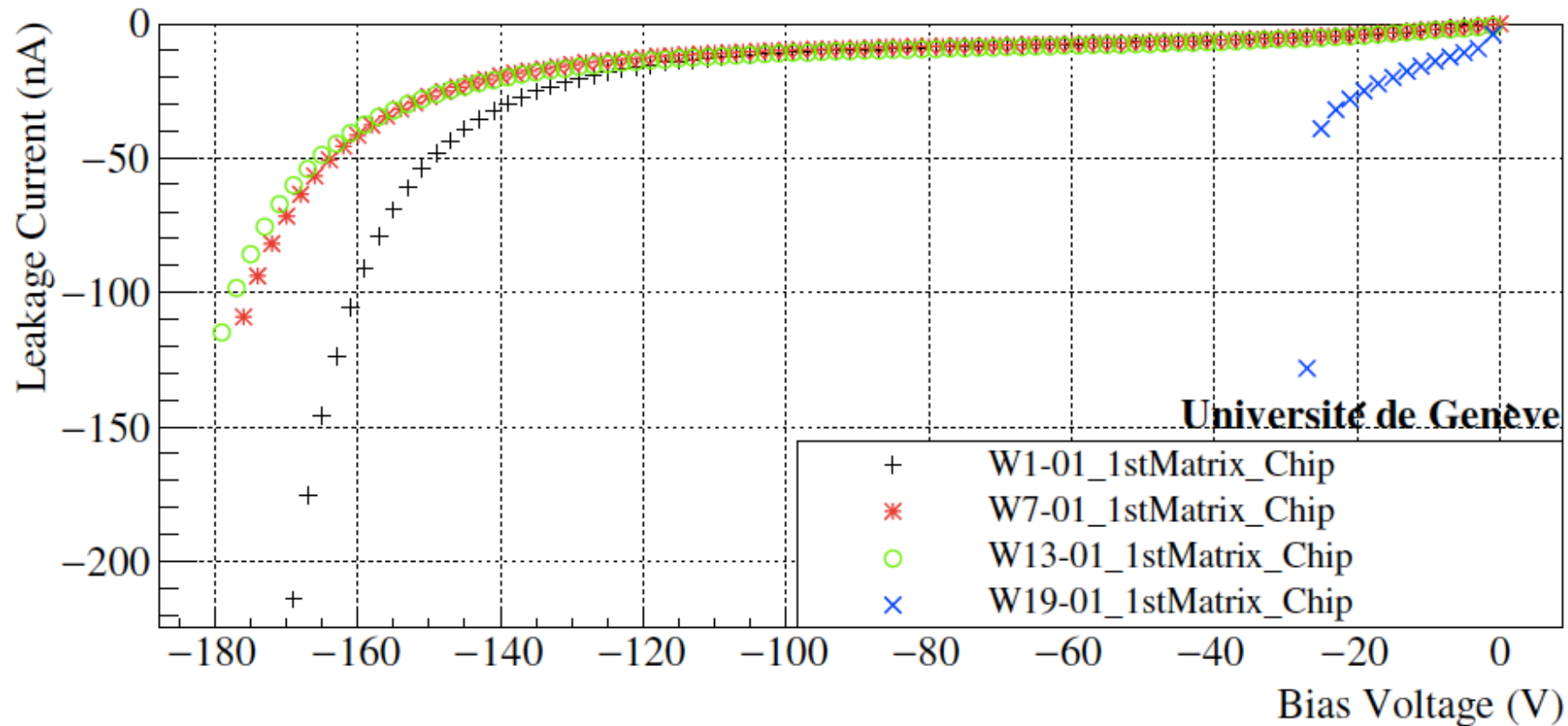

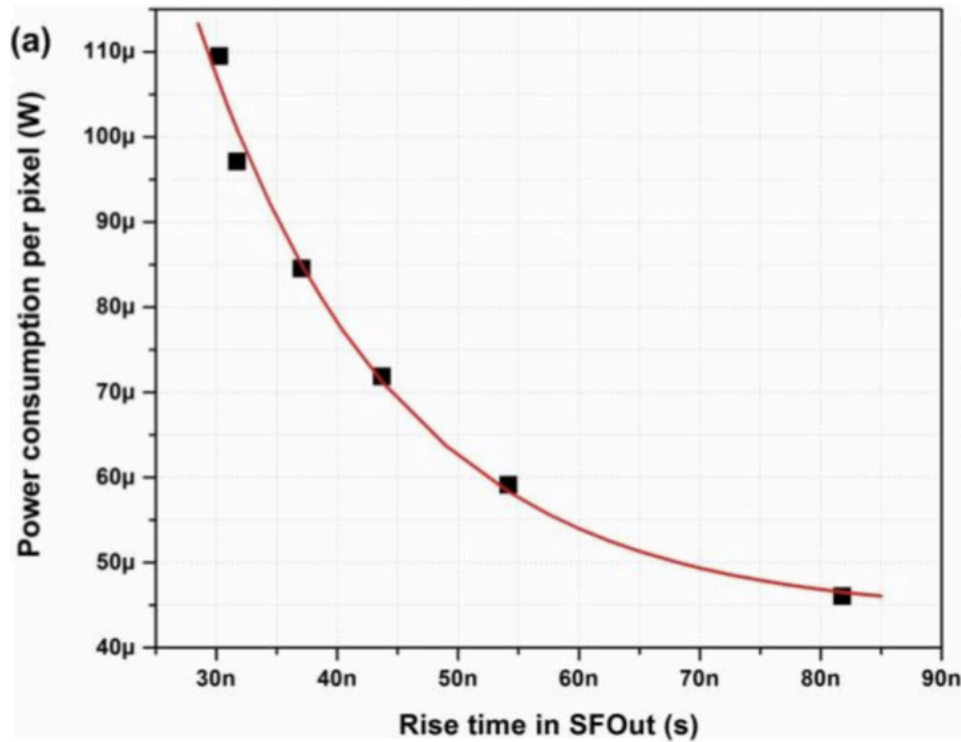- Consistent residual shape and width after alignment and tracking with Judith

50 µm pitch

250 µm pitch

Tails due to the large integration time

W1: 20 Ωcm, W7: 80-100 Ωcm, W13: 200-300 Ωcm, W19: 1k-2k Ωcm

Leakage Current (nA)

Bias Voltage (V)

Université de Genève

+ W1-01_1stMatrix_Chip
✳ W7-01_1stMatrix_Chip
○ W13-01_1stMatrix_Chip
✕ W19-01_1stMatrix_Chip

Power vs. rise time

(a)

- Simulation of the power consumption as a function of the rise time for analog pixels with high gain
- For low gain pixels (-p-tub +extra capacitor) the rise time can go down to 20 ns with aggressive settings

Stefano Terzo (IFAE, Barcelona) - Pizza Seminar, 19/07/2017