

# Current status of external test pulse equalization



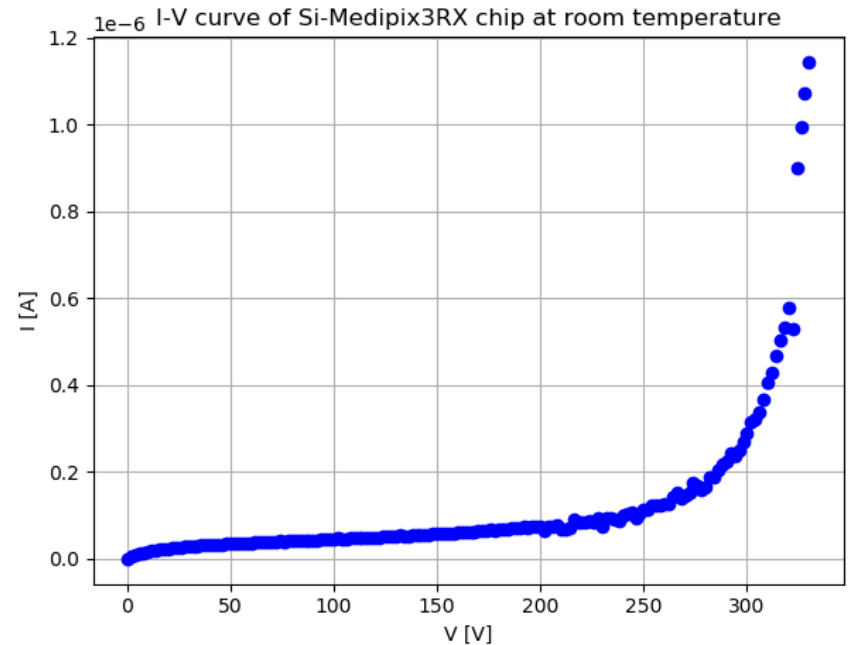
Adrián J. Suñer Rubio  
RIS3CAT project meeting

# Introduction

## IV Curve

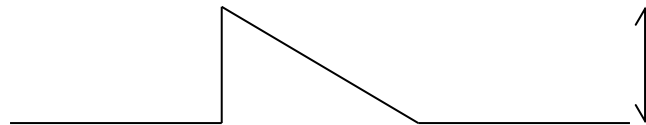
### Chip in study

Type	Wafer	ID
Medipix3RX	Silicon	7FB1FE72



### External test pulses

Type of pulses:

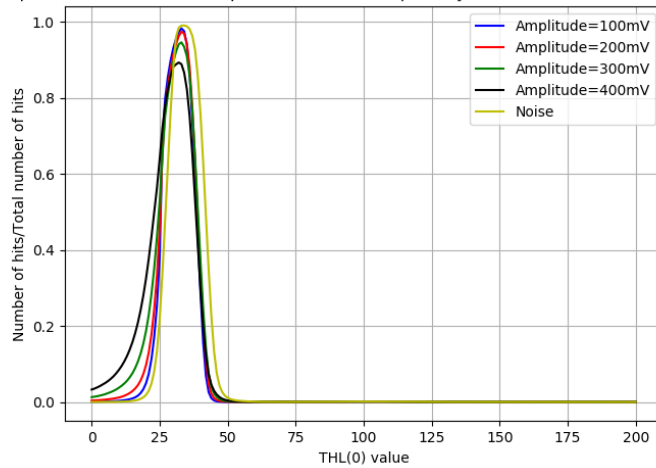


Amplitude= 0.1, 0.2, 0.3, 0.4, 0.5, 1, 2, 3 V

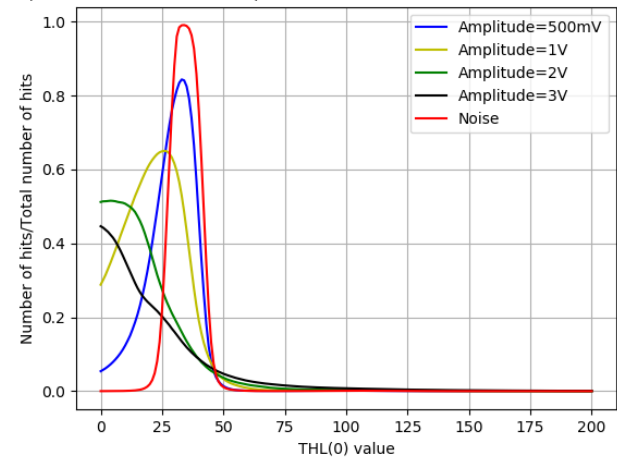
# External test pulses

Variation of the amplitude:

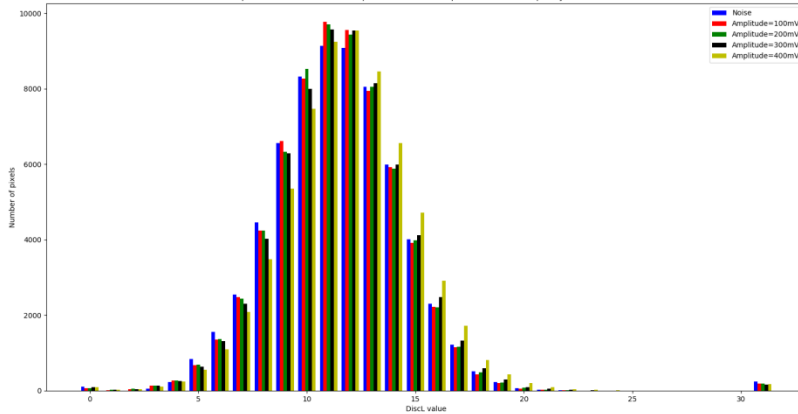
Equalization with external pulses of 10kHz frequency for Si detector with HV at 50V



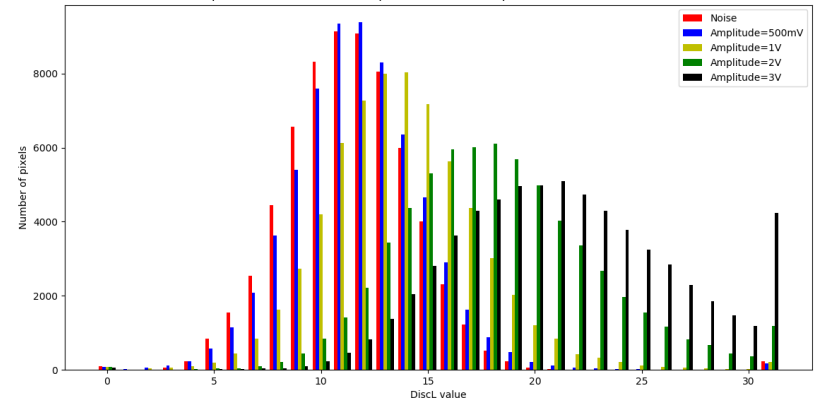
Equalization with external pulses and noise for Si detector with HV at 50V



Comparison of Discl. values to equalize with external pulses of 10kHz frequency with HV at 50V



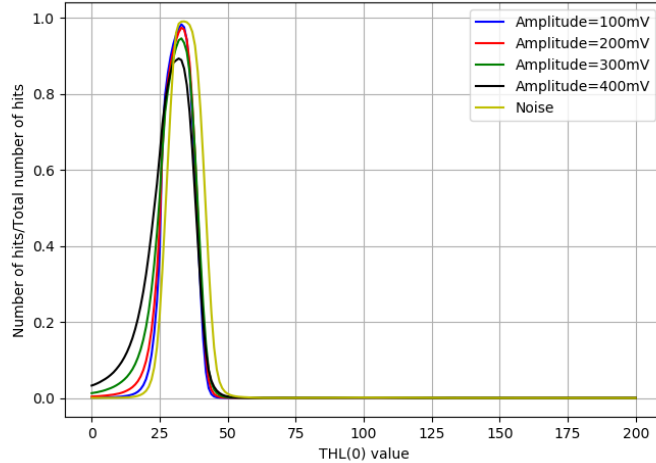
Comparison of Discl. values to equalize with external pulses and noise with HV at 50V



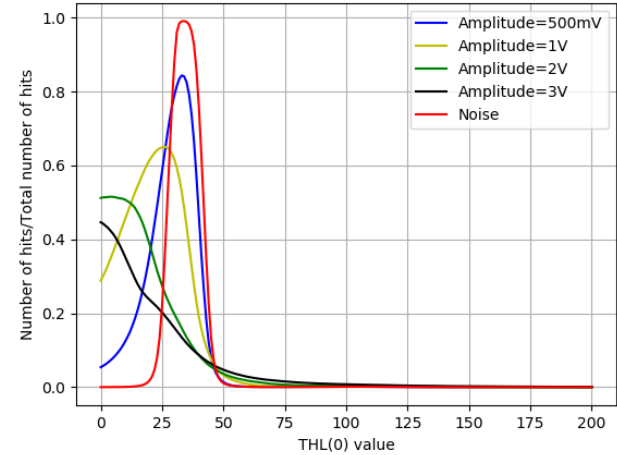
# External test pulses

Variation of the amplitude:

Equalization with external pulses of 10kHz frequency for Si detector with HV at 50V

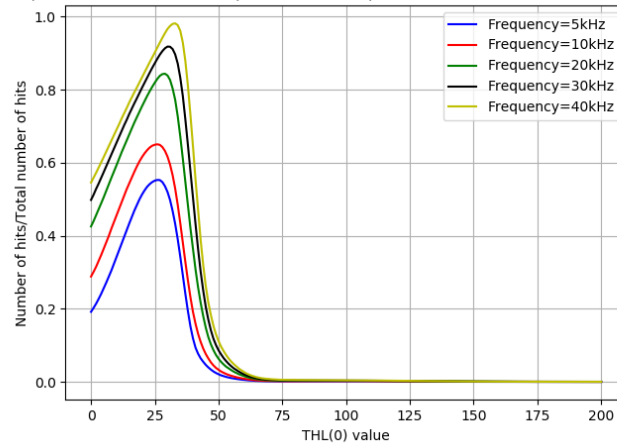


Equalization with external pulses and noise for Si detector with HV at 50V



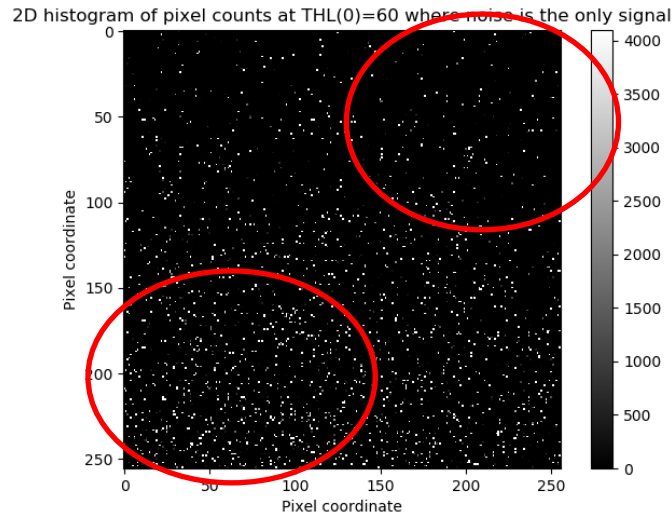
Variation of the frequency:

Equalization with external pulses of 2V amplitude for Si detector with HV at 50V

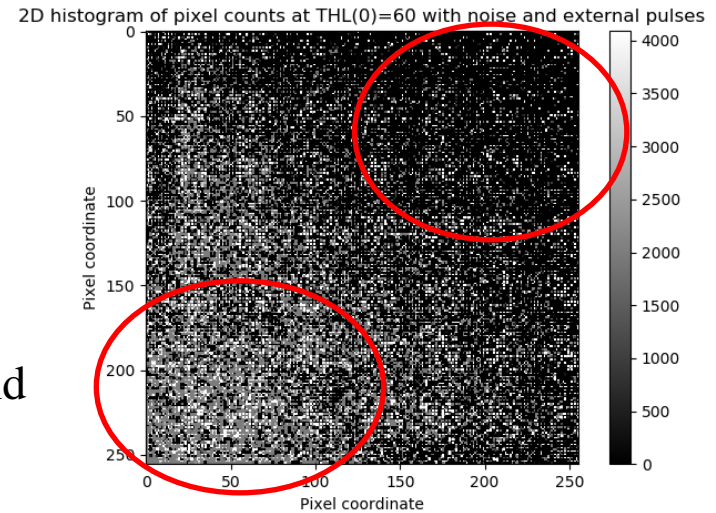


# External test pulses: Problems

Acquisition with noise



Acquisition with external pulses and noise



←→  
↓  
Same  
regions and  
shapes!

The problems may come from:

- Chip
- Injection of the pulses



Comparing both acquisitions the  
problem may be on the chip!  
(difference in the bump bonds, ...)

# External test pulses: Problems

## Acquisition with external pulses and noise

